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Design Checklist for Electronic Schematics and PCB Layouts

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Abstract: Guideline and checklist for development and drawing of electronic circuits, schematics and PCB layouts. Focus is on issues critical for system reliability, stability, testability and production often neglected and rarely covered by text books. Some specials regarding the usage of the CAE tool EAGLE¹ are also touched.

Keywords: device models, PCB, library, ratings, Boundary Scan, JTAG, IEEE1149.1, jumper, designators, values, numbers, net class, placement, alternative fitting, DFT, SMD, THT, reset, power-up, power cycling, FPGA, CPLD, pull resistors, unused pins, floating pins, ESD, vector font, prototype, solder stop lacquer, shorts, track width, temperature, thickness, drill size, connectors, via, pad, reference marks, German, English, translation, DRC, ERC, polygons, airwire, I²C, pull-resistors, dynamic, static, rise/fall time, silk screen, width, Gerber Data, drill, tolerances

¹ EAGLE is a registered trademark of CadSoft Computer GmbH.

1 Introduction

By providing this checklist I let my customers participate in my expertise I have been collecting over years as design and test development engineer. Some points of this work probably do not appear in most textbooks.

I do not intend to address academic problems of electronics but fairly simple rules that get neglected or forgotten during schematics and PCB design. Taking those rules serious much wasting of time and money can be avoided.

The line spacing throughout this document is left intentionally large to give the reader space for personal notes.

Special thanks to A. Zaffran at CadSoft Computer GmbH at <http://www.cadsoftusa.com> for the tables in the appendix. They have been written in German. A translation table from German to English keywords can also be found there.



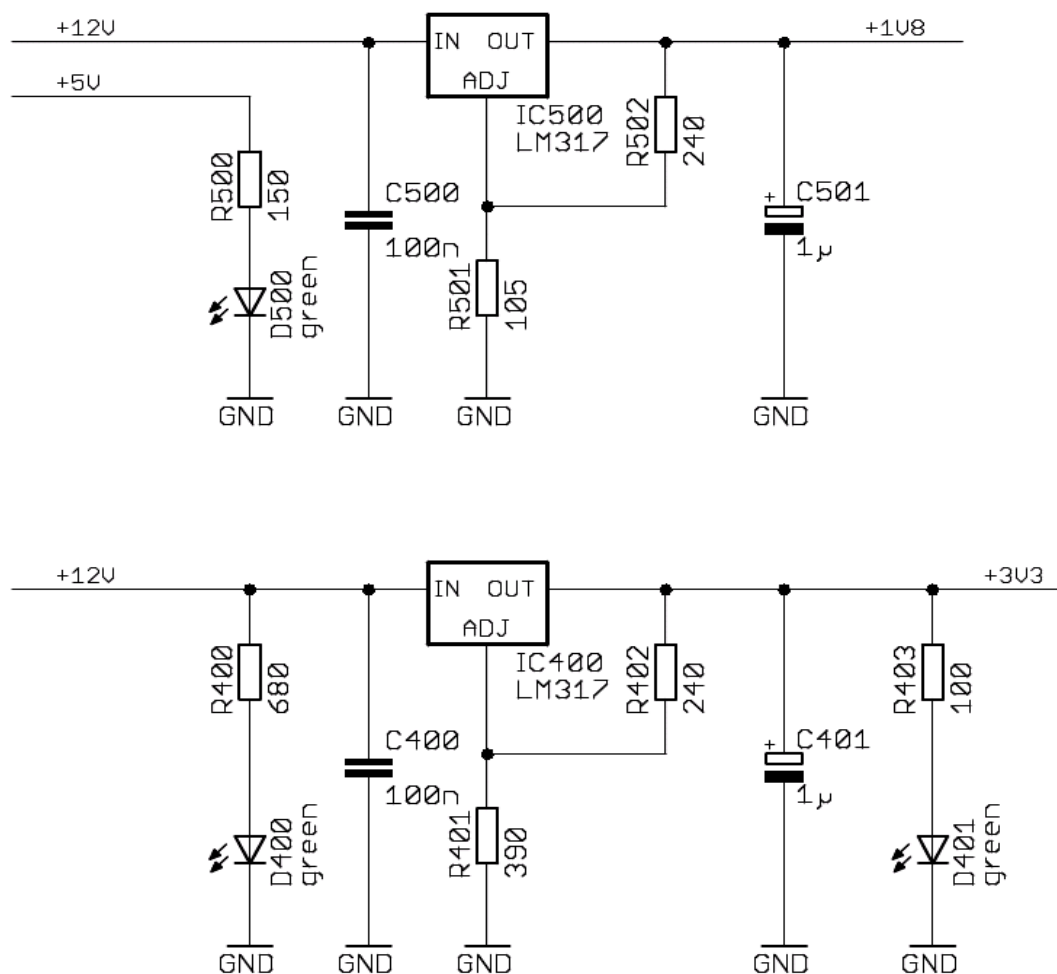
I appreciate all of critics to improve the quality of this document !

Contents

1 Introduction.....	2
2 Schematic.....	4
2.1 CadSoft EAGLE specific.....	23
3 PCB Layout.....	25
3.1 Prior to routing.....	25
3.2 While routing.....	31
3.2.1 Solder stop lacquer / mask.....	33
3.2.2 Polygons.....	34
3.2.3 Silk Screen Issues.....	36
3.2.3.1 Overlaps with Pads.....	36
3.2.3.2 Text Line Width (Ratio).....	37
4 Appendix.....	41
5 Useful Links.....	49
6 References.....	52
7 Disclaimer.....	52

2 Schematic

1. Verify the pinout of your device models in the CAD library !
 - ◆ Manufacturers of CAD / CAE systems usually do not guaranty 100% correctness!
 - ◆ Please be cautious when importing third party device models.
2. Do the device numbering group wise in relation to their function !
 - ◆ This eases the later process of PCB design and hardware debugging.
 - ◆ See following example: Devices needed to provide the +1,8V supply are numbered with R5xx, C5xx or IC5xx, whereas devices for the +3.3V supply have numbers greater than 400. *CadSoft* provides an ULP that performs this re-numbering in a convenient way: `renumber-sheet.ulp`



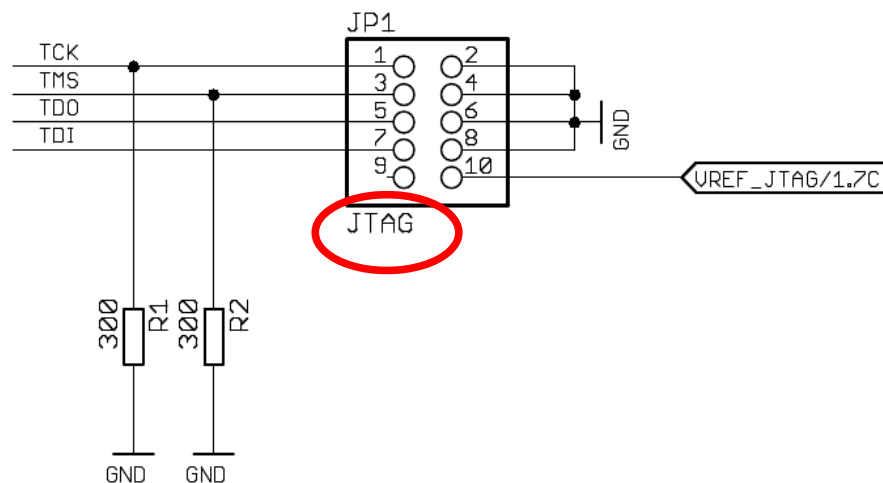
Drawing 1: numbering devices

3. Give all devices unambiguous values like 100R/2W or 10 μ F/35V ?

- ◆ By mere copying of devices wrong or ambiguous values may get spread around the schematic.
- ◆ Especially the **maximum allowed voltage** of capacitors or the **power rating** of resistors gets special attention this way. For example a series resistor for a standard 20mA LED operated at 12V may dissipate up to 0,2W heat !
- ◆ Avoid white-spaces in device values. They may confuse CAD data importing tools for JTAG/IEEE1149.x or other ATE. CAD data importing processes frequently understand a white-space as separation character in net – and partlists. **EAGLE does not forbid white-spaces in values !²**

4. Give connectors unambiguous values !

- ◆ E.g. the pin head JP1 should get a value that speaks for its purpose like „JTAG“.

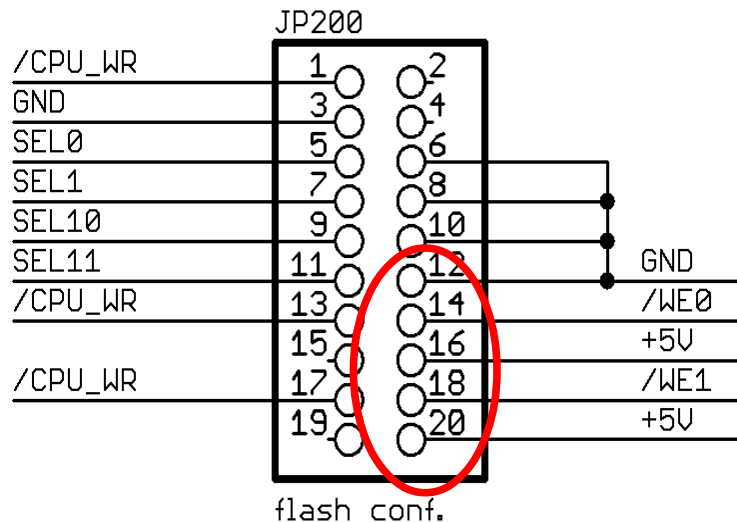


Drawing 2: connector values

² I recommend to CadSoft to output an ERC warning in such cases.

5. Do the connections to pinheaders so that there can **not** be a damaging jumper position !

- ◆ In the example below an inadvertent dangerous short from +5V to GND is impossible.



Drawing 3: no danger of power shorts at jumpers

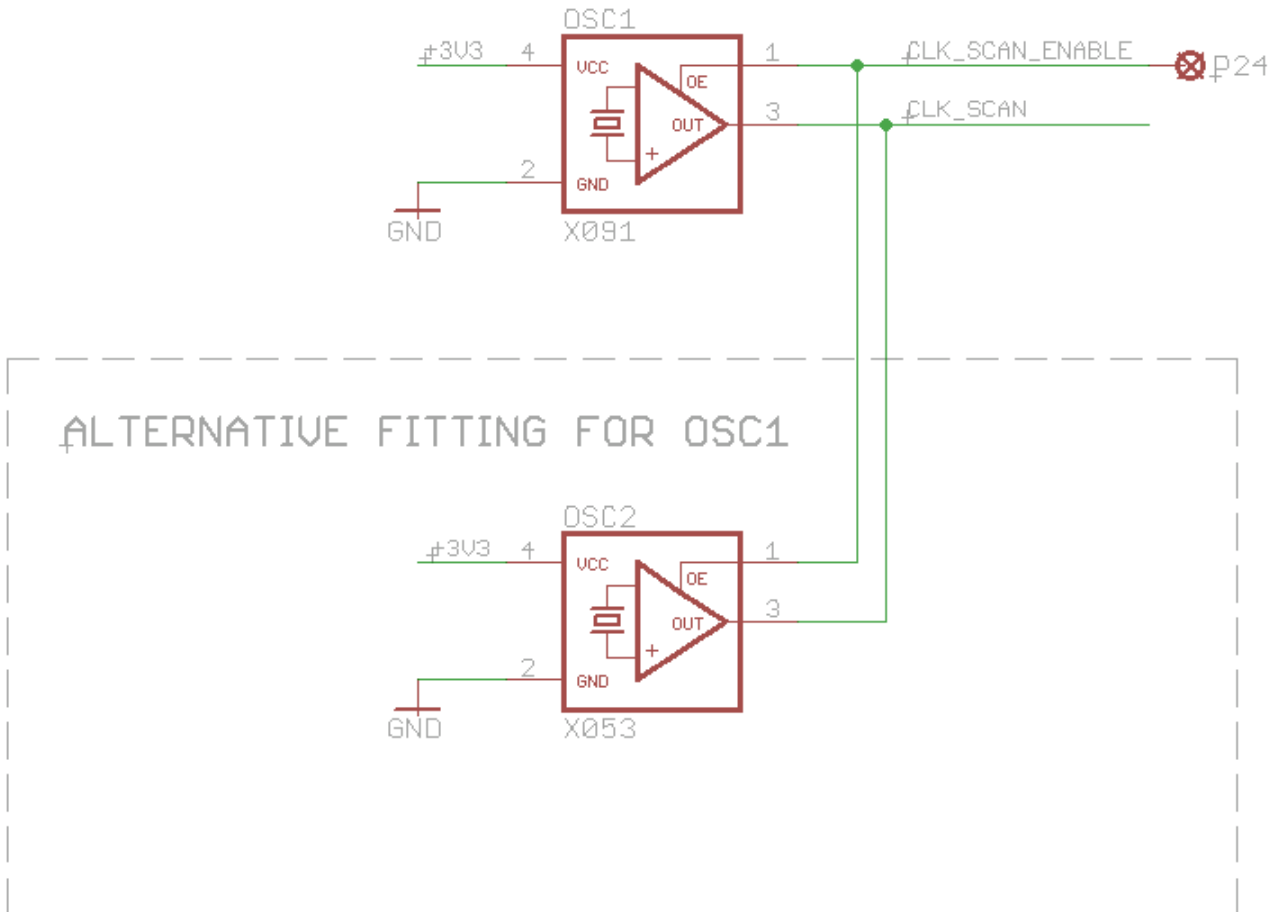
6. Give unambiguous designators to your devices !

- ◆ E.g. the designator „555“ for an IC is not always clear. An LM555 is not necessarily the same as an NE555 (compare datasheets).

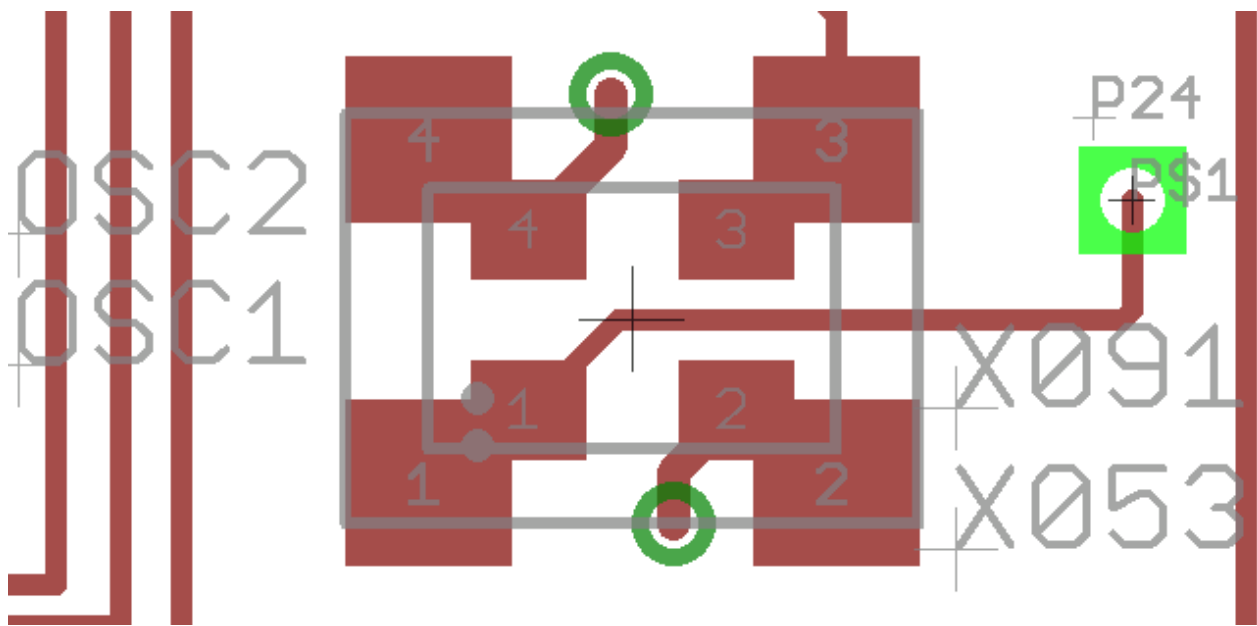
7. Take precautions for alternative fitting of devices !

- ◆ Time is running fast today. The production of a *top, super fast, cheap, high performance, ...* IC made for the mass market may become discontinued after 5 years so that you should have a *plan B* ready without the need to change the PCB layout.
- ◆ Component manufacturers notify about the device production status by words like **full production, not for new designs, obsolete, ...**
- ◆ Be also ready for delivery shortages of components.

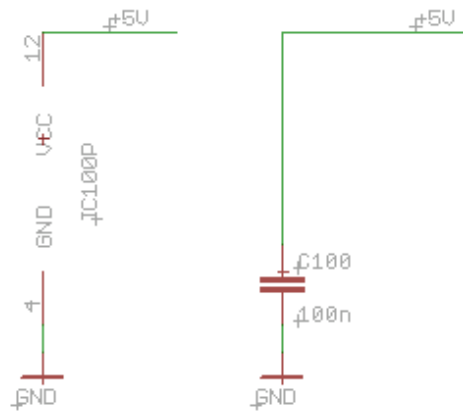
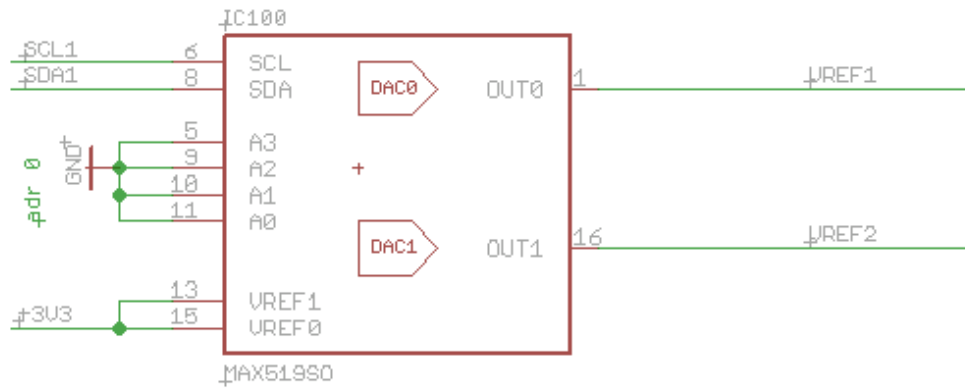
- ◆ In case the alternative components has a footprint differing from the original one: Draw in your schematic the alternative device parallel to the original one: Draw in your schematic the alternative device parallel to the original device and leave a text note for your colleges (see Drawing 4 to 8).



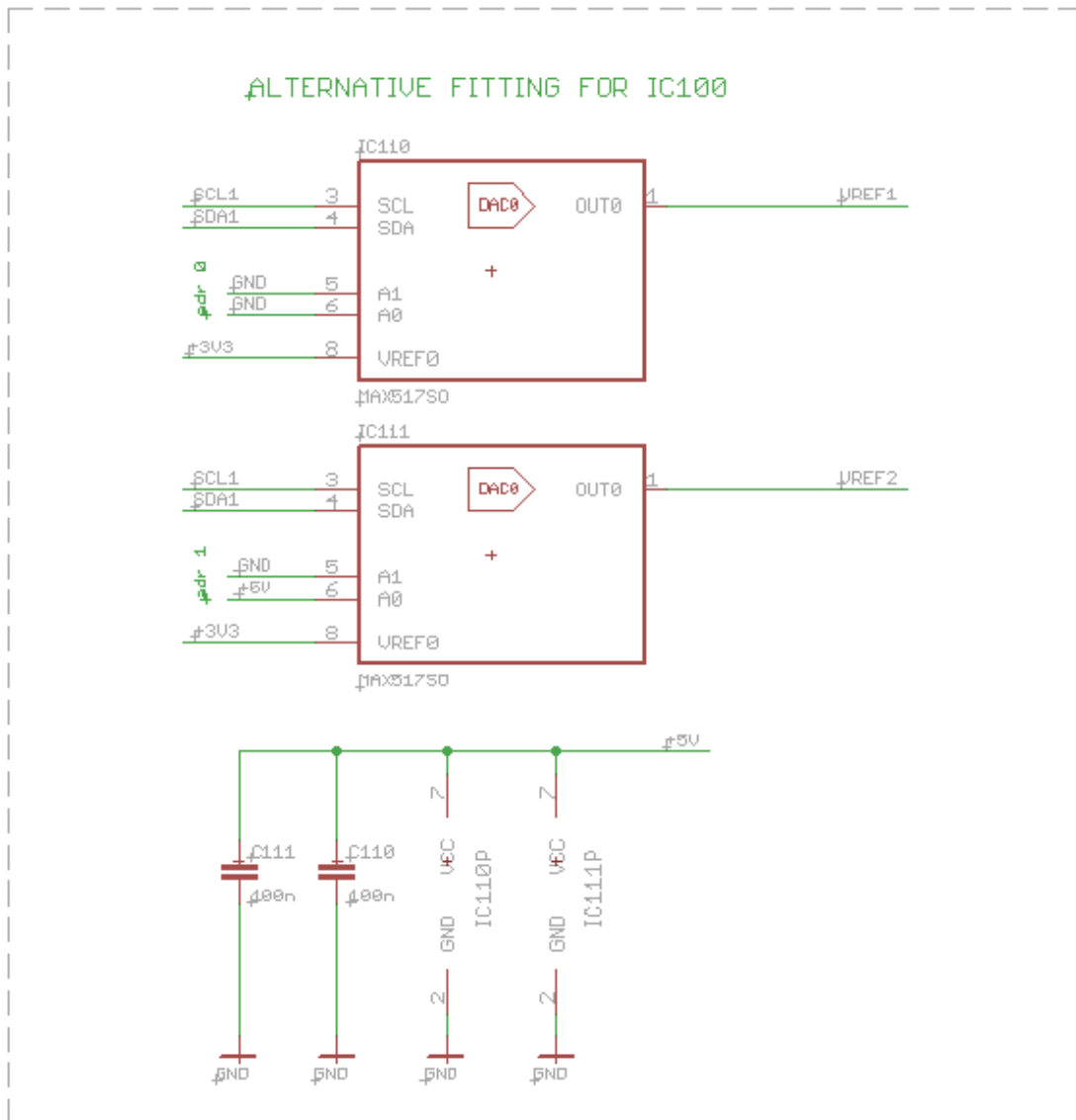
Drawing 4: alternative fitting in schematic



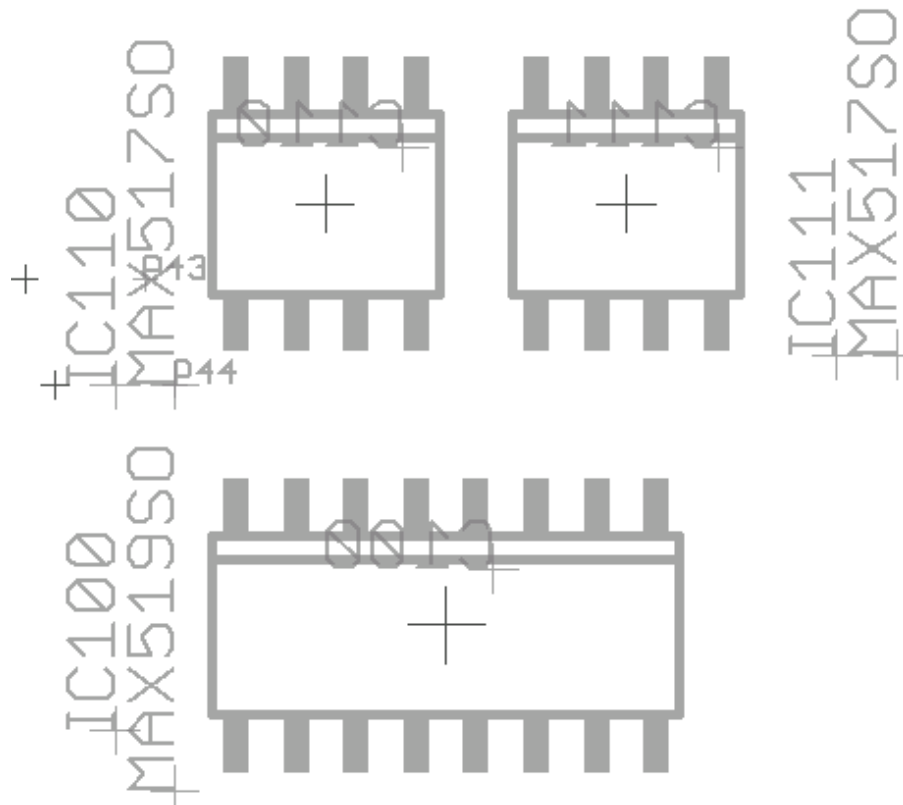
Drawing 5: alternative fitting on PCB



Drawing 6: alternative fitting in schematic



Drawing 7: alternative fitting in schematic



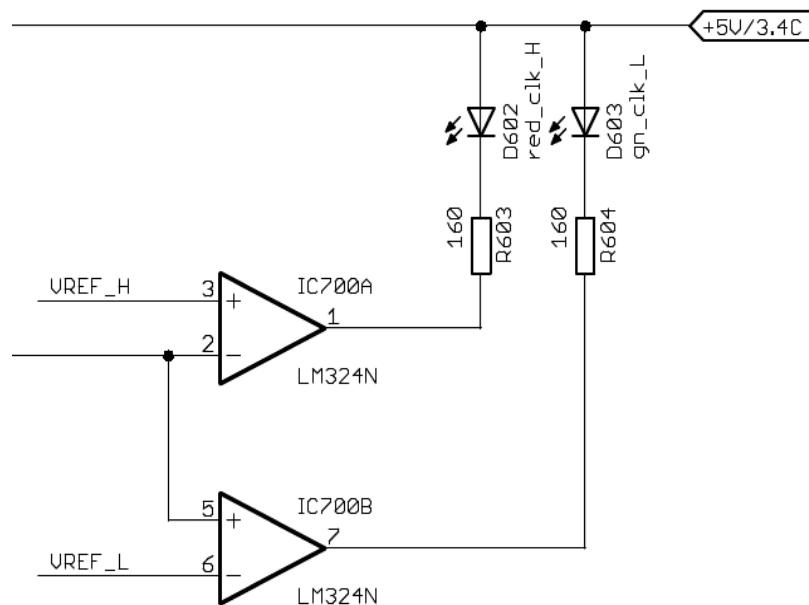
Drawing 8: alternative fitting on PCB

8. If you intend to have the board assembled manually please consider the person doing the job !
- ◆ Use as **less different** values as possible. For example assembling a board with 20 resistors of 10kOhms each is faster and less error prone than a board having 3 x 8,2k , 7 x 12k, 5x 9,5k and 5x 10k.
 - ◆ This eases ordering and purchasing the components (**Prices** fall as the ordering amount increases usually).

9. Does your circuitry also work stable and reliable if
- ◆ optional components are not fitted ?
 - ◆ connectors are open for a period of time ? Inputs of ICs may **float free**.
 - ◆ Do **not** entirely rely on the ERC (Electrical Rule Check) of your design tool in this case !
10. Does your circuitry behave predicable during reset or power cycling ?
- ◆ **Note:** During reset the I/O pins of CPLDs, FPGAs, processors and controllers go HIGH-Z or may drive HIGH ! In this phase nets may **float** or cause **dangerous conditions** you have never thought of before like a motor driver bridge shorting VCC and GND.
 - ◆ While in reset state or during power cycling collisions may occur. Outputs may drive against each other. Bus contention on wide bus systems does pose stress to driving devices and leads to increased thermal load on them.
 - ◆ Does your circuitry perform a proper reset after power-up ?
 - ◆ Do capacitors, especially of the reset circuitry, have a path to discharge after power-down ?
 - ◆ Do supply voltages reach their nominal value withing the maximum allowed time ?
 - ◆ Does the power-up sequence of supply voltages matter ?
 - ◆ Make sure the supply voltages die during **power-down** in a sequence that does not cause any damage. **The power-down period may last several seconds !** I recommend a signal – called /PWR_DOWN_ALL – that feds several critical voltage regulators and turns them of simultaneously during that time.
 - ◆ What is the behavior of **not-programmed** ICs like CPLDs, FPGAs after power-up ? For example the I/O pins of the Xilinx Coolrunner II are pulled high by internal resistors of minimal 40kOhm against VCC_IO.
 - ◆ What is the behavior of **programmed** ICs like CPLDs, FPGAs after power-up ? In the fitter options of [ISE at www.xilinx.com](http://www.xilinx.com) the power-up value of registers may be set.

11. Inputs and Outputs of ICs

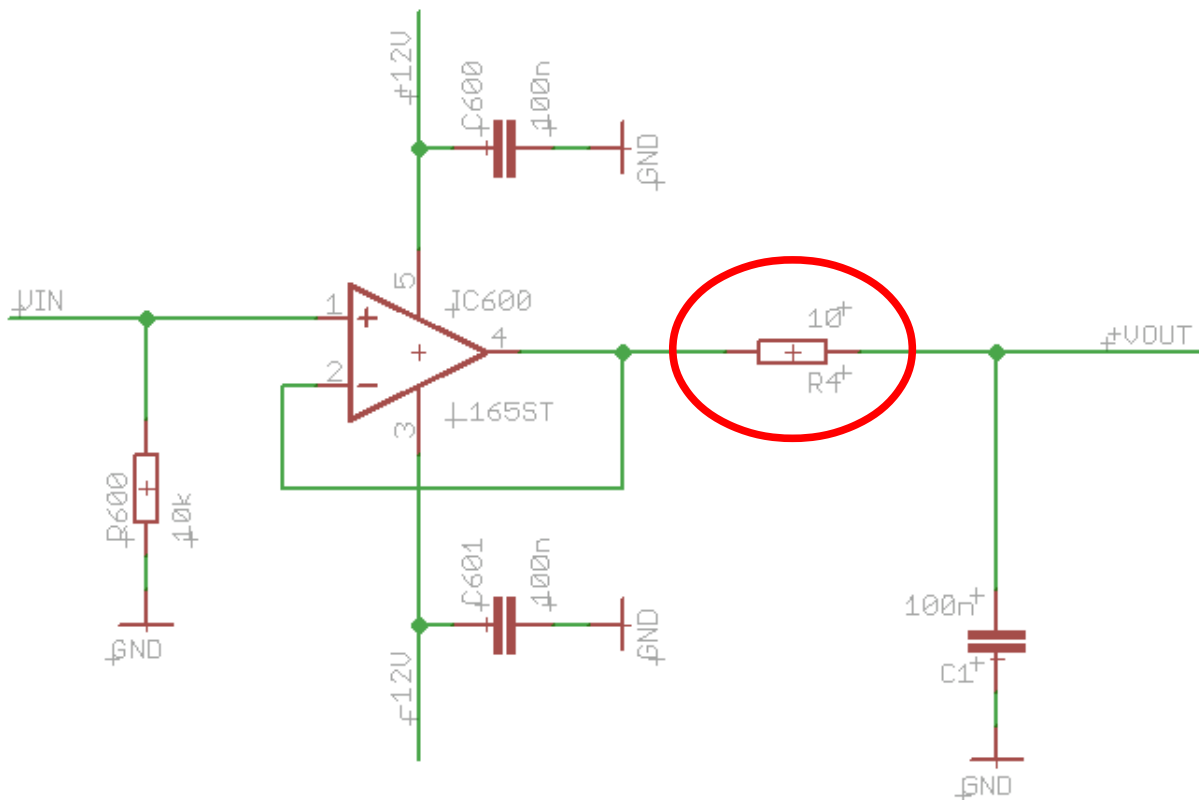
- ◆ Is the load at outputs within safe range – even in case of alternative fitted components ? Even if there is no overload, the voltage at outputs changes under load. Digital downstream inputs may not read the state properly in such cases as shown in the example below: The outputs of the operational amplifiers fall to around 1V sinking the LED currents (provided a single supply voltage of the Op-amp). 1V is hard to be interpreted as L signal for downstream devices.



Drawing 9: op-amp sinking current

- ◆ Do (non-FET) operational amplifiers have DC current paths from their inputs to GND ?
- ◆ Are drivers (like CMOS drivers) capable of driving (multiple) inputs of downstream ICs. Especially mixing of digital device families may lead to “misunderstandings” among them. (See datasheets for output/input voltage ranges, fan out/in) ?

- ◆ Make sure pull-resistors are within manufacturer specified range. If their value (resistance) is too high, the static performance of the line might be okay, but the dynamic switching will be outside the specified range (rise/fall time negatively impaired). If the value is too low, driver pins might be overloaded or line voltages might shift outside safe ranges. Pay attention to specifications of I²C devices.
- ◆ Operational amplifiers may drive **negative** voltages (when supplied symmetrical) to (digital) downstream devices which may get stressed or damaged in such a case.
- ◆ Avoid **capacitive loads** at op-amp outputs ! Op-amps with feed back loops tend to instability if capacitive loaded. Workaround: Add a series resistor right after the op-amp output to isolate the downstream capacitors (Drawing 10).



Drawing 10: op-amp with isolated capacitive load

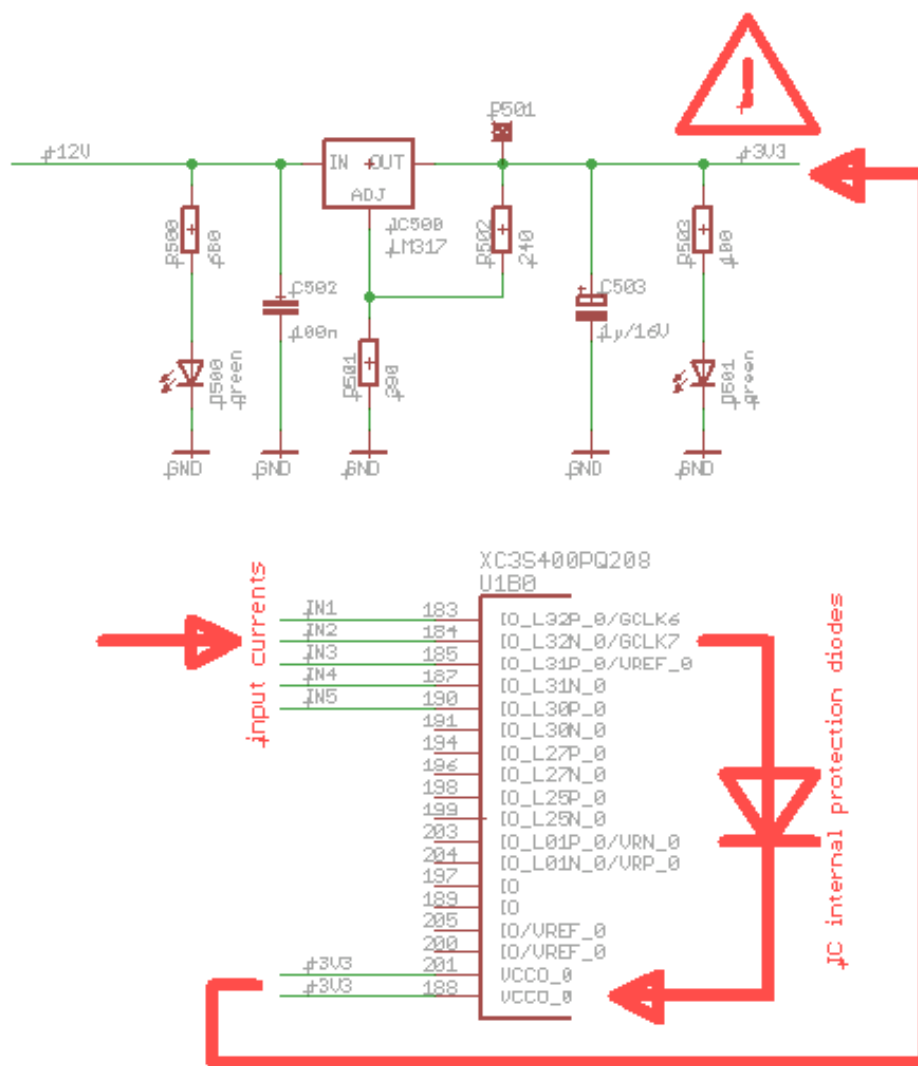
- ◆ Are LH or HL edges of digital signals short enough ? Digital devices show **miraculous** behavior if fed with signals changing to slow. For example if you drive a digital clock input of an XC9572 CPLD by a slow operational amplifier like the well known LM324 you will encounter very strange effects...
- ◆ In harsh industrial environments an output (at a connector) may get shorted inadvertently. Does the driver survive this load at all ? Please take your time to consider this scenario. Replacing the whole unit at customers site may get more expensive than the time you spend thinking on this matter.
- ◆ Probably ESD (electrostatic discharging protection) is an issue for you. *NXP* provides outraging solutions at <http://standardproducts.nxp.com/> .

12. I²C issues

- ◆ If an I²C slave is to solely receive data (like a DA-Converter) implement a software procedure/function that verifies that the SDA line is **not shorted** to GND. If SDA is shorted to GND for some reason, the I²C master will always see the SDA line low, thus misinterpreting the stuck-at-low SDA as acknowledge bit sent by the slave. The acknowledge bit is the **only means** to verify at a **low level** that the I²C slave is properly connected to the master.

13. Backdriving

- ◆ If ICs inputs are driven with voltages exceeding the specified maximum ratings given by the manufacturer, backdriving occurs. More or less current flowing into the inputs will accumulate and drain into the power rail, thus raising the voltage there.
- ◆ Most voltage regulators do **not** sink current into their outputs. So there is danger of **damaging** other devices "living" from the affected power rail.



Drawing 11: backdriving into power rail

14. Make sure digital ICs are fed with patterns clearly allowed by the manufacturer !

- ◆ Example: The pattern HLL driven into the inputs A, B and C of an IC causes the device to behave **unpredictable** on its outputs. If you can't avoid such a situation, does it impair the system performance or cause dangerous effects ?

15. Has a minimum of address pins of (FLASH)-EEPROMs been connected ?

- ◆ Example: When programming or just ID code reading of a W29C020 a succession of 5555h, 2AAAh, ... on the address bus is issued by the processor on at least 15 address lines ! If you tied address pins 15..12 low, because you don't need them in normal mode, the device could not be programmed in-system later on !³

16. JTAG / IEEE 1149.x

- ◆ Provide termination resistors to GND on TCK and TMS. I recommend from experience to have 300 Ohms each (see Drawing 2 page 5).
- ◆ Do the boundary scan system (or JTAG-system) drivers have sufficient strength to make a reliable H level on TCK and TMS when loaded with 300 Ohms ? When doing **system level test**, TCK or TMS pins of several boards are to be driven in parallel which reduces the resistive part of the transmission line far below 300 Ohms !
- ◆ Provide an optional pull-up resistor on TDO of **each** IC on the UUT/ Target-System. ICs not fully compliant to IEEE1149.1 may lack this resistor internally. Not fitting an external TDO pull-up resistor makes less headache than adding one later with airwires and glue...
- ◆ May the optional L-active **asynchronous** Test-Reset (/TRST) signal become required some time ? Even if your Scan System does not drive the /TRST signal – always have it accessible via a testpad or a jumper ! **Never** tie /TRST hard to VCC or GND !
- ◆ Layout GND connections generously (see Drawing 2 page 5).

3 This is a very rare case but it indeed happened to me once.

- ◆ Provide means of **switching scan paths** (jumpers, Scan Path Linkers, Scan Bridges, ...). For example while system programming the scan chain should be as short as possible (IEEE1149.7 relieves you from that because it allows star topology of scan paths). Another scenario: Optional not fitted ICs within the scan path cause breaks in a serial chain – therefore provide solder bridges between TDI and TDO of the device affected in order to close the break.
- ◆ Alternatively, devices needed for in system programming may be placed in a separate scan path. Short scan paths → less programming duration → lower production **costs** !
- ◆ /WE, /RD or /CE signals should be wired to pinheaders or jumpers to allow driving them by the boundary scan system externally. This way in system programming can be sped up to a large extent. Optionally provide buffers if these signals are to be distributed among multiple UUTs.
- ◆ Programming adapters of programmable logic manufacturers may require a reference voltage provided **by the UUT** (see Drawing 2 page 5), whereas boundary scan systems may **output** a voltage to supply the UUT. Make sure these voltages can't get shorted.
- ◆ Make sure the clock of synchronous RAM ICs can be driven by a boundary scan capable pin in test-mode. Usually in non-test-mode the RAM clock is driven by a PLL or other clock generators. Provide means to “bypass” or disable the PLL in test-mode.
- ◆ Boundary Scan Test systems frequently classify devices during CAD-import **by value**⁴. *Example 1: A single resistor is classified as such by its value 5k1 which is fine so far. If there was a resistor network/array with the same value the CAD-import may output garbage. Make sure no other devices - except single resistors - in your design have the value 5k1 too ! I strongly recommend to give resistor arrays values like 8x5k1 or 8_5k1.*
Example 2: Capacitors of value 100pF may get just a 100 as value for convenience. Imagine the trouble if there are 100 Ohms resistors with just the

⁴ This way of classifying devices is a result of speeding up test setup time. I'm not in favor of this practice since it brings some risks along.

value 100 ? The scenarios described here occur most frequently but similar cases are also easy to imagine.

- ◆ Pay attention to special pins which determine the IC's test-mode behaviour. Especially some FPGAs have pins like /DONE, PROG or Mode-pins (e.g. M0, M1, M2) which need to be held at a certain level in order to allow full Boundary Scan Test access. Some CPUs require a certain number of clocks applied at TCK while other configuration pins (like a reset input or a mode input) must be high or low for that period of time. I recommend pull-resistors or at least test pads there. In special cases a connection to a connector might be required. Please read the datasheets and BSDL-files carefully !
- ◆ While in test-mode, I/Os may behave different from the full-operational mode. For example, the XILINX Spartan 3 FPGA, pulls all I/Os down via internal resistors. Together with external pull-up resistors, the result is a voltage divider. Thus, the voltage at the pin may be outside of specifications, which results in unpredictable test results.
- ◆ There might be a pre – and a post configuration BSDL file required for some ICs ! The post-configuration BSDL should be output by the logic synthesis tool.
- ◆ Does power sequencing matter ? (see point 10 page 12)
- ◆ Provide means for a full galvanic separation of the scan path signals (incl. GND) from the scan master.
- ◆ Avoid driving the scan path signals into the UUT when powered down.
- ◆ Provide means to monitor and limit the power consumption of the UUT.
- ◆ See reference (7) Mario Blunk, “A Guide to test methods and why to go for Boundary Scan” at http://www.train-z.de/bsm/how_to_test.pdf for more.

17. Design for Test (DFT)

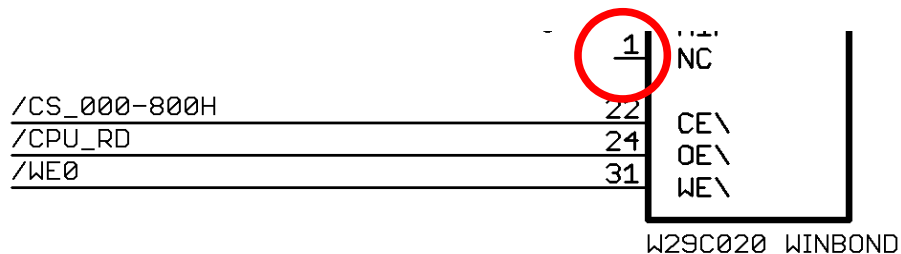
- ◆ **Note:** Your product will make it to series production some time.
- ◆ Care for safe, fast and easy testing of the board in advance !
- ◆ Contact PCB and assembly houses during board design.
- ◆ If the majority of devices is of analog nature the board is likely to be tested by

ICT (In-Circuit-Test) or manually. Have you provided test pads on critical signals ? Also have a look at drawings 14 and 15 on page 22.

- ◆ Multilayer boards fitted with BGA packages usually don't allow **mechanical access** to signals !
- ◆ Digital areas of the board should be tested by Boundary Scan/JTAG according to IEEE1149.1/6/7. See point 16 page 17 .

18. Make unused IC pins accessible.

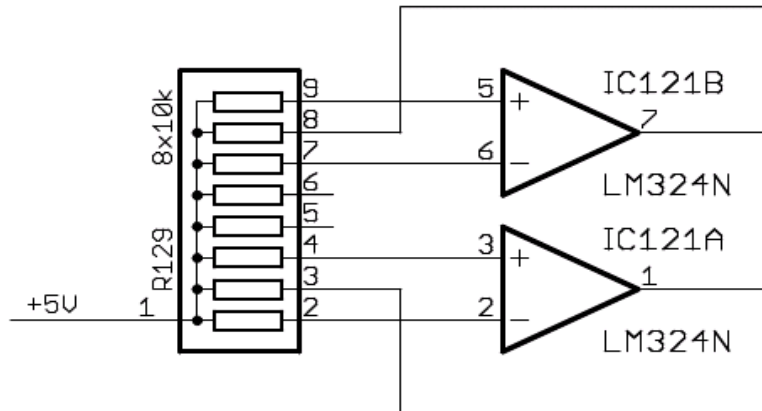
- ◆ Do not just hard wire them to GND or leave them open as this makes extensions or modifications difficult or impossible.
- ◆ This also applies for pins that are named with NC or “no connect”. NC means: *The pin is not bonded or wired inside the IC.* In case there will be a **replacement** by a similar device later, this pin may become important. See following example: A successor of the W29C020, an AM29F040 has pin 1 serving as address input A18. If left open in the original design (where it was an NC pin), the successor IC would have A18 floating free – **fatal !**⁵



Drawing 12: NC pins may become a problem

⁵ Some datasheets do not allow to connect NC pins at all, which makes in-advance-connecting of NC pins impossible.

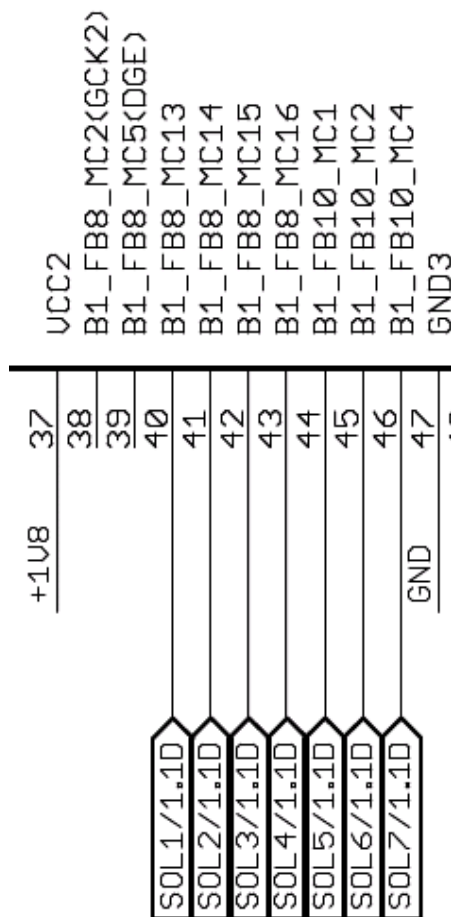
- ◆ The next example shows two left over operational amplifiers of a quad Op-amp (LM324). Should there be a modification later they are accessible since they are “soft” wired via R129.



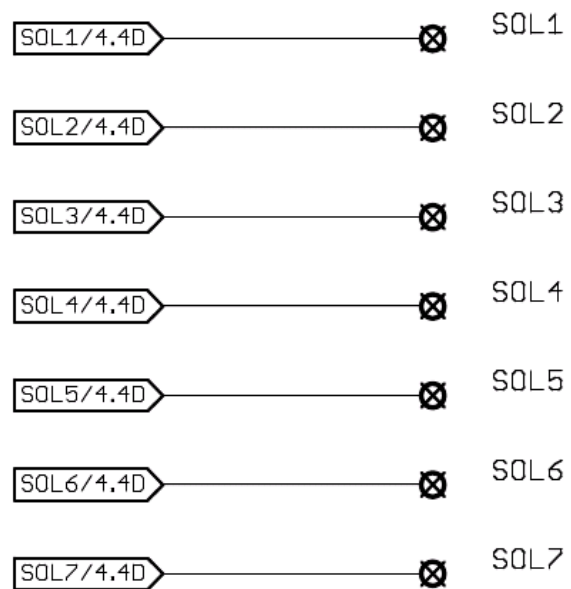
Drawing 13: soft wiring of leftover op-amps or gates

- ◆ If you also wire these pins with solder pads or pin header mechanical access becomes simple. Apply this method when using fine pitch packages like TQFP-144 or BGAs.
- ◆ I also recommend to wire these pins with pull resistors externally.

- ◆ The example below (left hand) shows 7 unused pins of a Xilinx Cool-Runner which have been wired to solder pads (right hand).



Drawing 14: solder pads



Drawing 15: solder pads

19. Have you named **all** nets explicitly ? Even those without **label** ?

- ◆ Just relying on automatic naming of your design tool does not give much of value as far as later board debugging goes. E.g. a net name „CATHODE_RESET_LED“ does say more to your colleague than just „N\$1701“.

20. Have you defined **net classes** ?

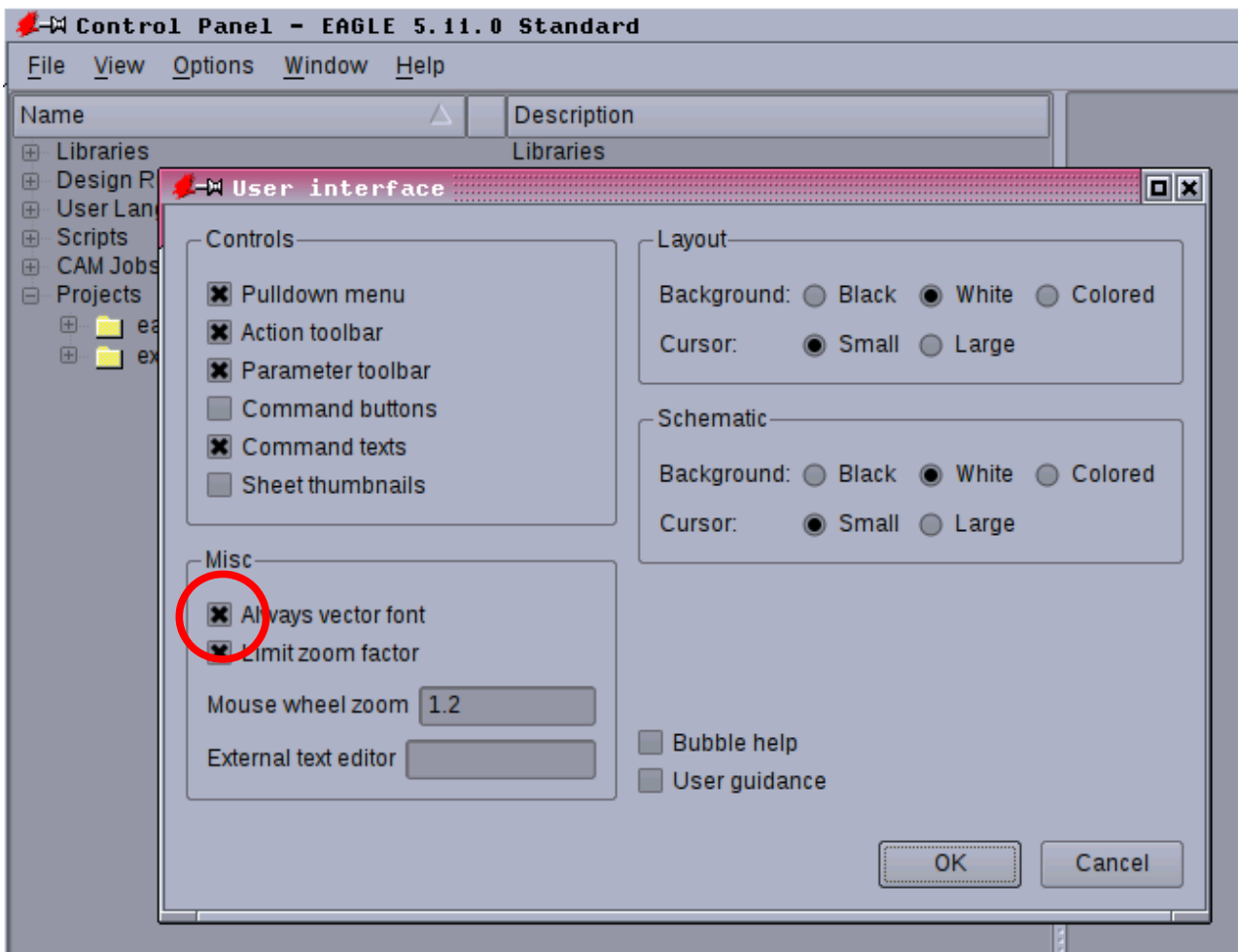
- ◆ For later layout design its important to define track widths and clearances of certain nets **in advance**.
- ◆ Contact your PCB house as far as minimal structure dimensions goes.

2.1 CadSoft EAGLE specific

There are various parameters like fonts, text sizes, text ratio, line widths etc. that can be preset so that you are not required to do all these settings all over again when starting a new project. To make things easy just take the file [eagle.scr](#) provided in section 5 point (2).

1. I recommend to **always** use **vector font**.

- ◆ Vector font guaranties constant text size independent of zoom when printing on paper.
- ◆ Vector font is also required for production of your PCB as varying text size may result in **shorts** when using proportional font in copper layers.
- ◆ By default vector font is **disabled** in *EAGLE*⁶.
- ◆ By the way, vector font looks much more professional ...

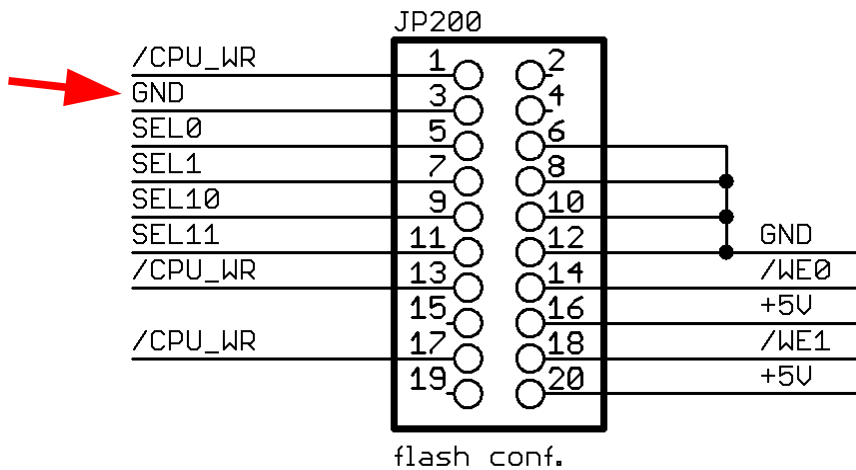


Screenshot 1: always enable vector font

6 I recommend CadSoft to make vector font default.

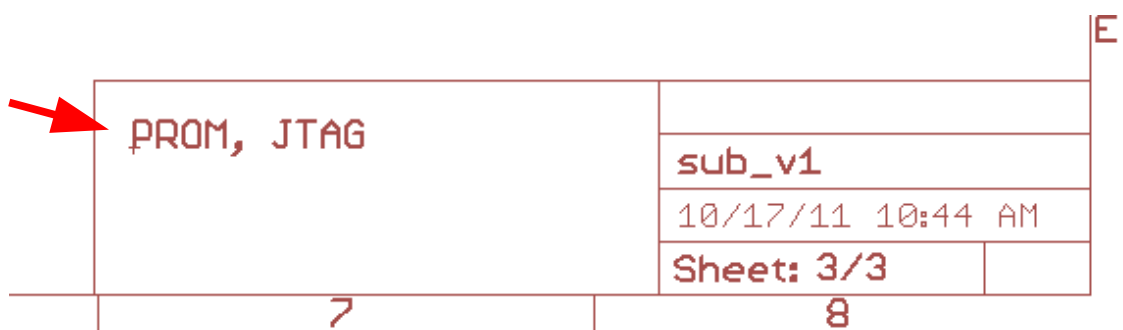
2. Text size

- ◆ I recommend to place net labels with size 0,05 inch or 50 mil (Drawing 16).
- ◆ If nets are crossing pages, make use of so called Off-Page-Labels (Drawing 15 page 22). These labels indicate the page and coordinates where the respective net re-appears in the schematic.



Drawing 16: net labels

- ◆ Texts located in the doc field should be of size 0,1 inch (Drawing 17).



Drawing 17: doc field

3. Do not forget to run the ERC from time to time during schematics design.

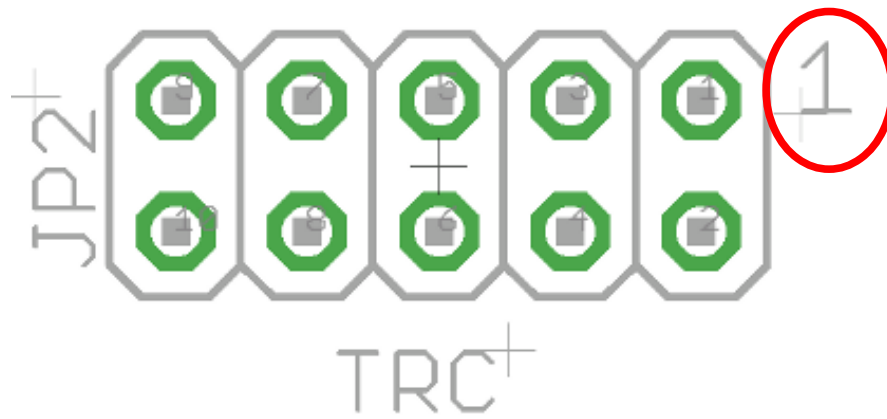
3 PCB Layout

3.1 Prior to routing

1. Check mechanical properties of your device models regarding:
 - ➔ package dimensions
 - ➔ drill sizes of pads (It's very disgusting if the pins of a screw clamp do not fit into the drills.). **Consider maximum drill tolerances guaranteed by your PCB house !**
 - ➔ Care for keep out areas (important with SMD packages) (layers 39 & 40 in CadSoft EAGLE).

2. mounting holes
 - ◆ Make sure the hole diameter (including tolerances) is correct.
 - ◆ Should there be an electrical connection to **protective ground** ?
 - ◆ Use the "lock" command to nail down holes so that they can't be moved inadvertently.

3. placing of connectors, jumpers, switches, LEDs, displays:
 - ◆ What are the requirements of the target application ?
 - ◆ **Your customer determines, not you alone !**
 - ◆ Have you marked pin 1 of connectors (Drawing 18) ?
 - ◆ Use the "lock" command to nail down these devices so that they can't be moved inadvertently.

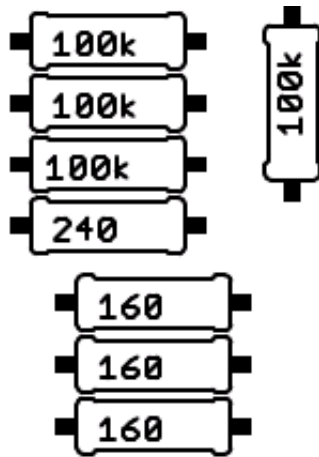


Drawing 18: mark pin 1

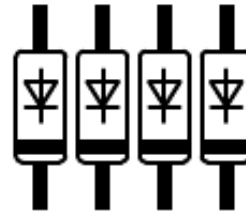
- ◆ Arrangements of multiple LEDs should have all the anodes pointing to the same direction (See 20). This goes for SMD diodes too !
 - ◆ Pin headers and connectors should have a clearance around so that the counterpart plugged there does not collide with other neighboring devices⁷.
 - ◆ If your target application poses mechanical stress on connectors, I recommend **not** to place them directly on the board as pads tend to get loose or ripped out. Place those connectors in the **housing walls** instead.
4. Make sure devices on top of bottom side do **not overlap** !⁸ Consider heat sinks and their accessories that usually require more space than you think.
5. In case you plan to **manually** assemble the board (even when using SMD): As a courtesy to your colleges consider following (as far as signal integrity allows of course):
- ◆ Resistors of equal value may be placed in groups.
 - ◆ Diodes and capacitors may be placed with their cathodes/poles pointing to the same direction.
 - ◆ These measures make the assembling less error prone, faster and **cheaper**.

⁷ Most THT packages shipped with the EAGLE library do not have a keepout frame.

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Drawing 19:



Drawing 20:

6. Board version, top / bottom side marking

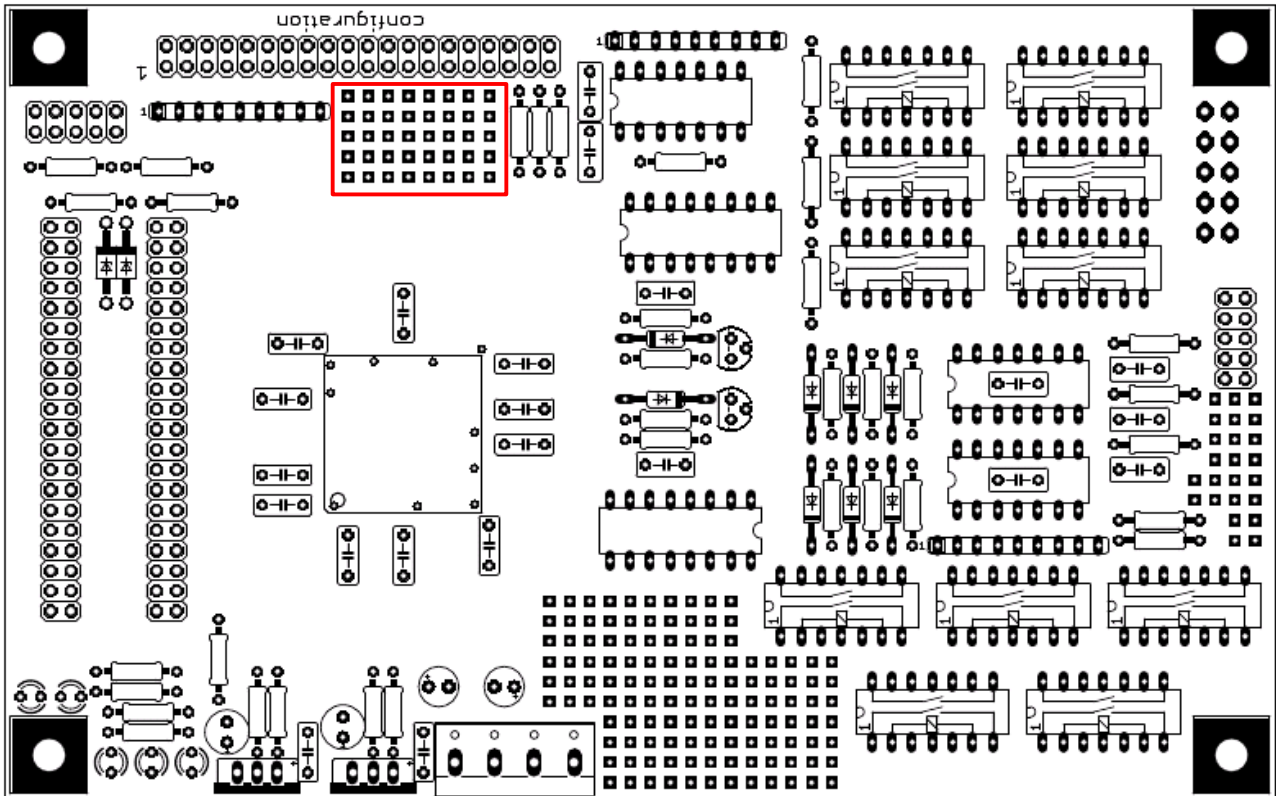
- ◆ Place a text in the copper like “top” or “bot” to identify sides
- ◆ Place board name/version in top or bottom side copper like “RS232-IF_V3.2b”

7. Reference marks

- ◆ Contact EMS house as how and where reference marks should be placed on the board. They are required by assembly and placing machines !

8. Solder pads for modifications or extensions

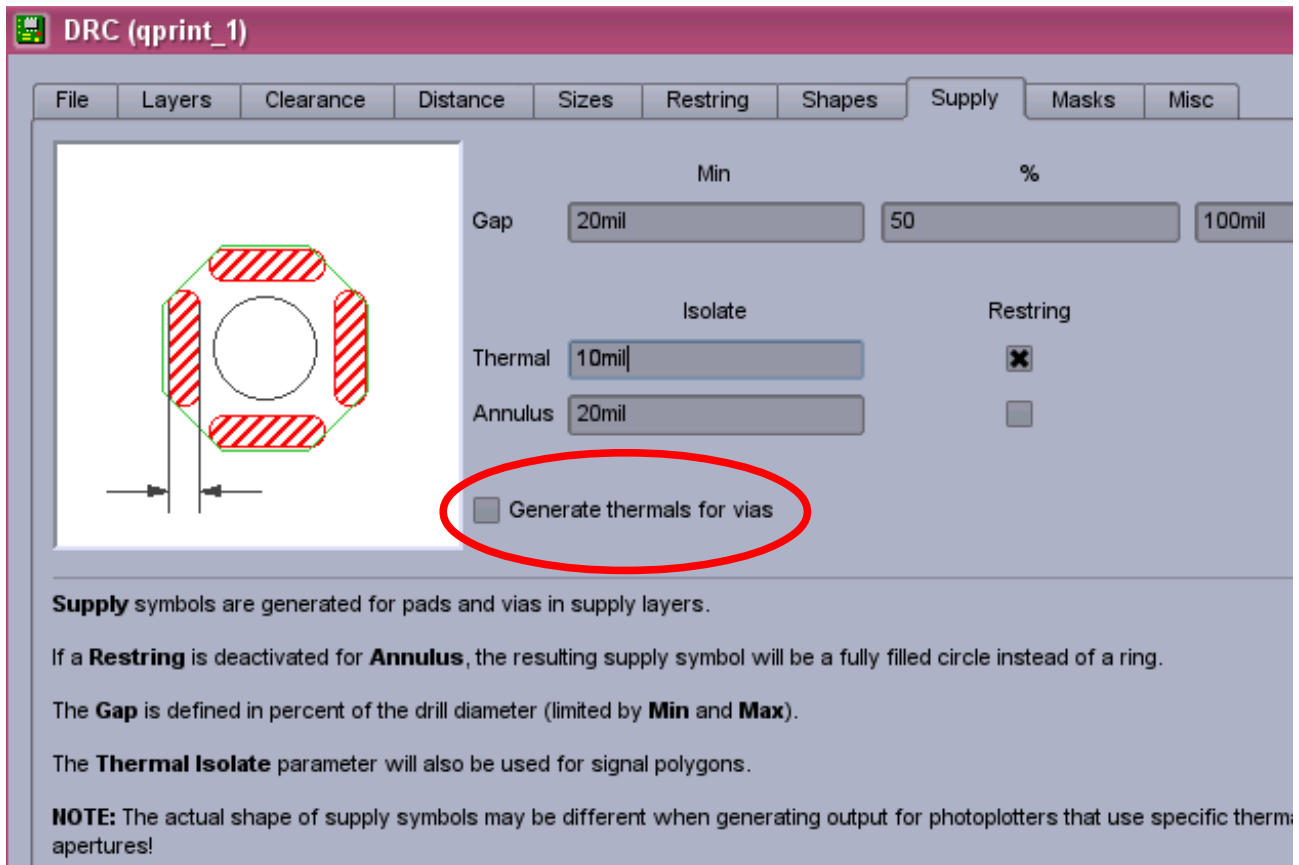
- ◆ When in prototype phase, you are required to make changes on your board like additional pull resistors or just a status LED. As precautions provide solder pads **in advance** as shown in the drawing below framed **red**.



Drawing 21: solder pad arrays

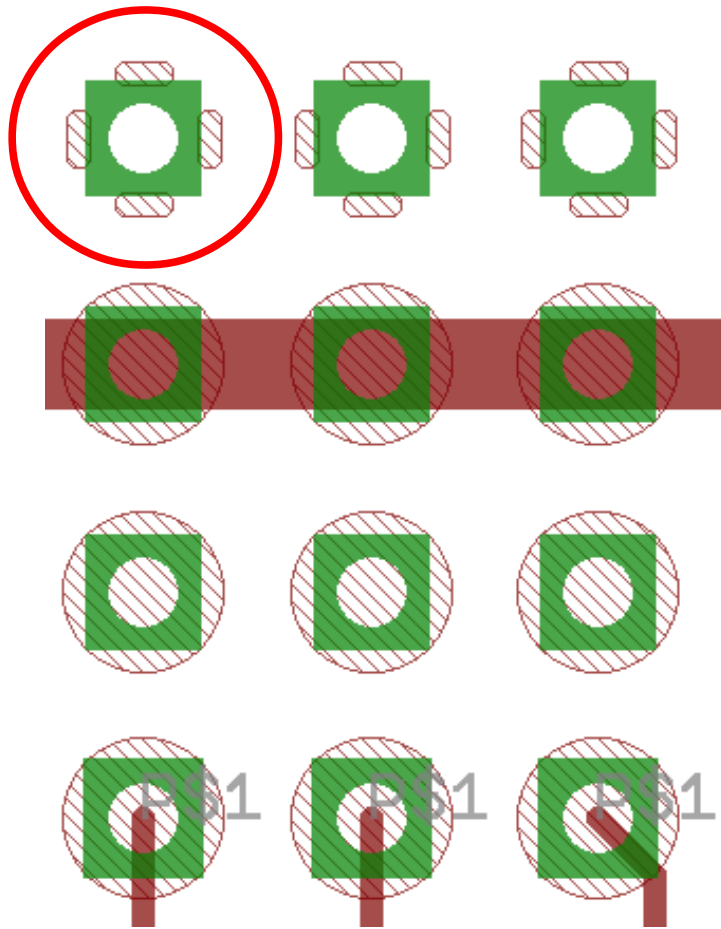
- ◆ Solder pad arrays of this kind can be made by pads or lots of vias. Pads, as shown in Drawing 15 page 22, are “real” electrical devices (with symbol and package). Vias can be placed in the board only. They do **not** have a counterpart in the schematic.

Note : Check the “via thermal” option in the DRC settings. This way vias become “solder able” . Otherwise they become connected to the surrounding copper plane which draws away all the heat that comes from the solder machine (screenshot 2).⁹



Screenshot 2: via thermal setting in DRC

⁹ This option does apply for inner layers only as these layers are allowed to be supply layers. Thus via thermals can not be created in “top” and “bottom” layers.

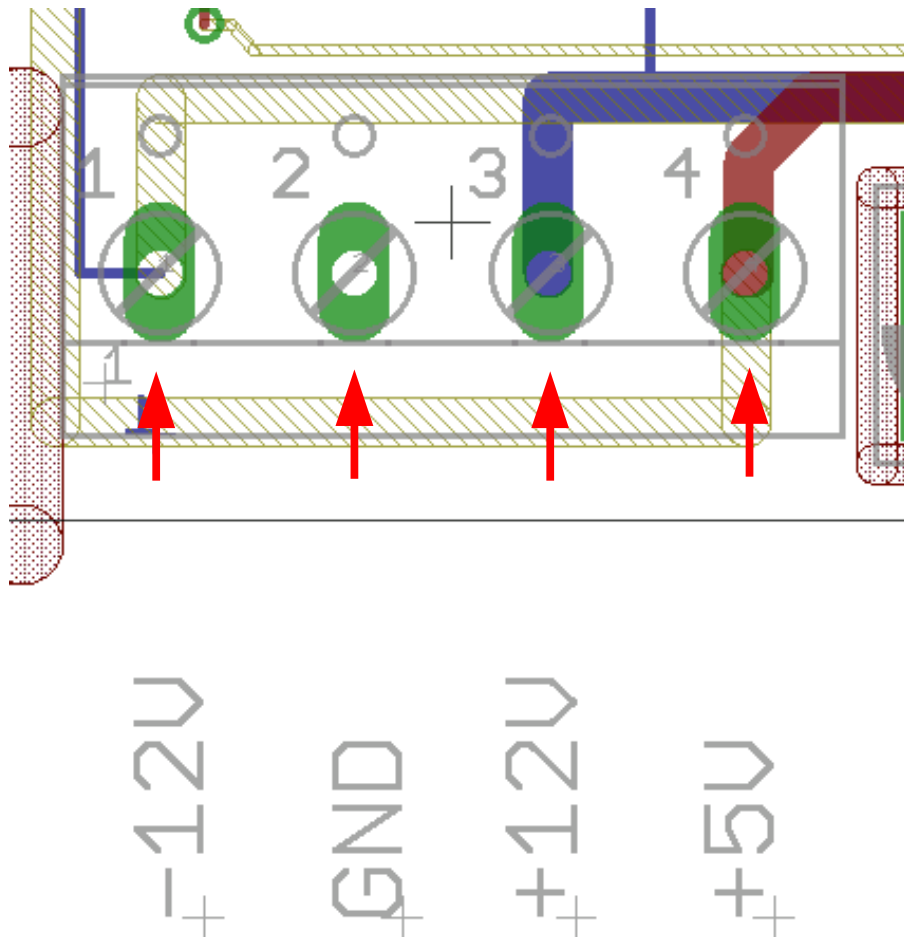


Drawing 22: via thermals in inner layers

- ◆ Modifications or extensions soldered there look relatively good and are of stable mechanical nature.
- ◆ See examples in Drawing 14 and 15 on page 22.

3.2 While routing

1. Run DRC from time to time and **finally** before sending the BRD-file to production !
2. Please consider the maximum current load of copper tracks (see Appendix).
 - ◆ Unavoidable **critical** conditions should not lead to **blown tracks**. See also section 2, page 12, point 10 In a harsh industrial environment an output may get shorted inadvertently temporarily.
3. Avoid vias inside a pad as the solder may drain into the via hole. The solder left on the pad may become too less for a reliable pin-pad joint. **Contact EMS house !**
4. In the proximity of screw clamps or connectors the board is probably going to be stressed heavily.
 - ◆ Avoid tracks in top layers where wires are inserted. In Drawing 23 the red arrows indicate the direction wires are inserted. They may **disrupt** a track or scratch the solder stop lacquer – **danger of shorts !**



Drawing 23: no tracks in top layer near a screw clamp

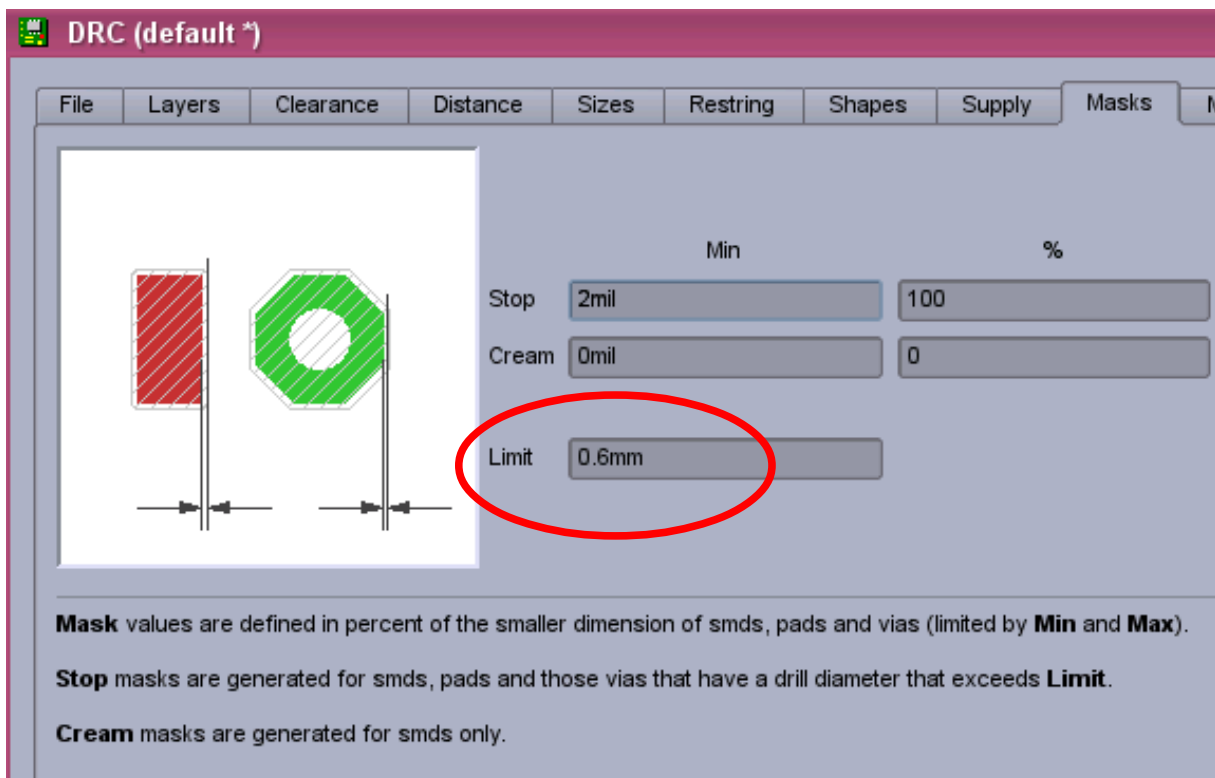
- ◆ Generously, as far as possible, provide copper areas on pads or mounting holes in order to improve mechanical stability. Usually device models provide just a minimum of copper around their pads.

3.2.1 Solder stop lacquer / mask

- ◆ Vias should be **covered** with lacquer always.

Note: If the board is to be **wave soldered** shorts between vias and pads may result otherwise !

- ◆ Keep vias free from lacquer in **exceptional** cases only. Drawing 3 gives an example of how to set this rule in the DRC menu: All drills with a size greater than 0.6mm do **not** become covered with lacquer¹⁰ and thus will be exposed for soldering. This applies for all vias.

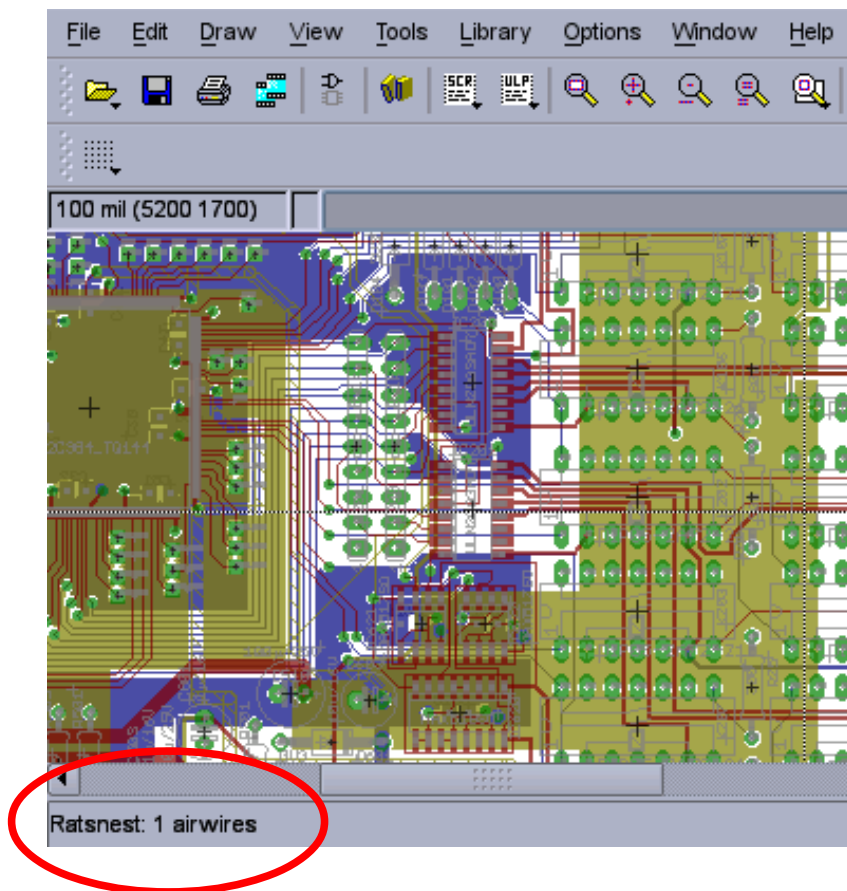


Screenshot 3: solder stop mask on vias

¹⁰ The default setting here is 0 mm. Means no drills are to be coated with lacquer.

3.2.2 Polygons

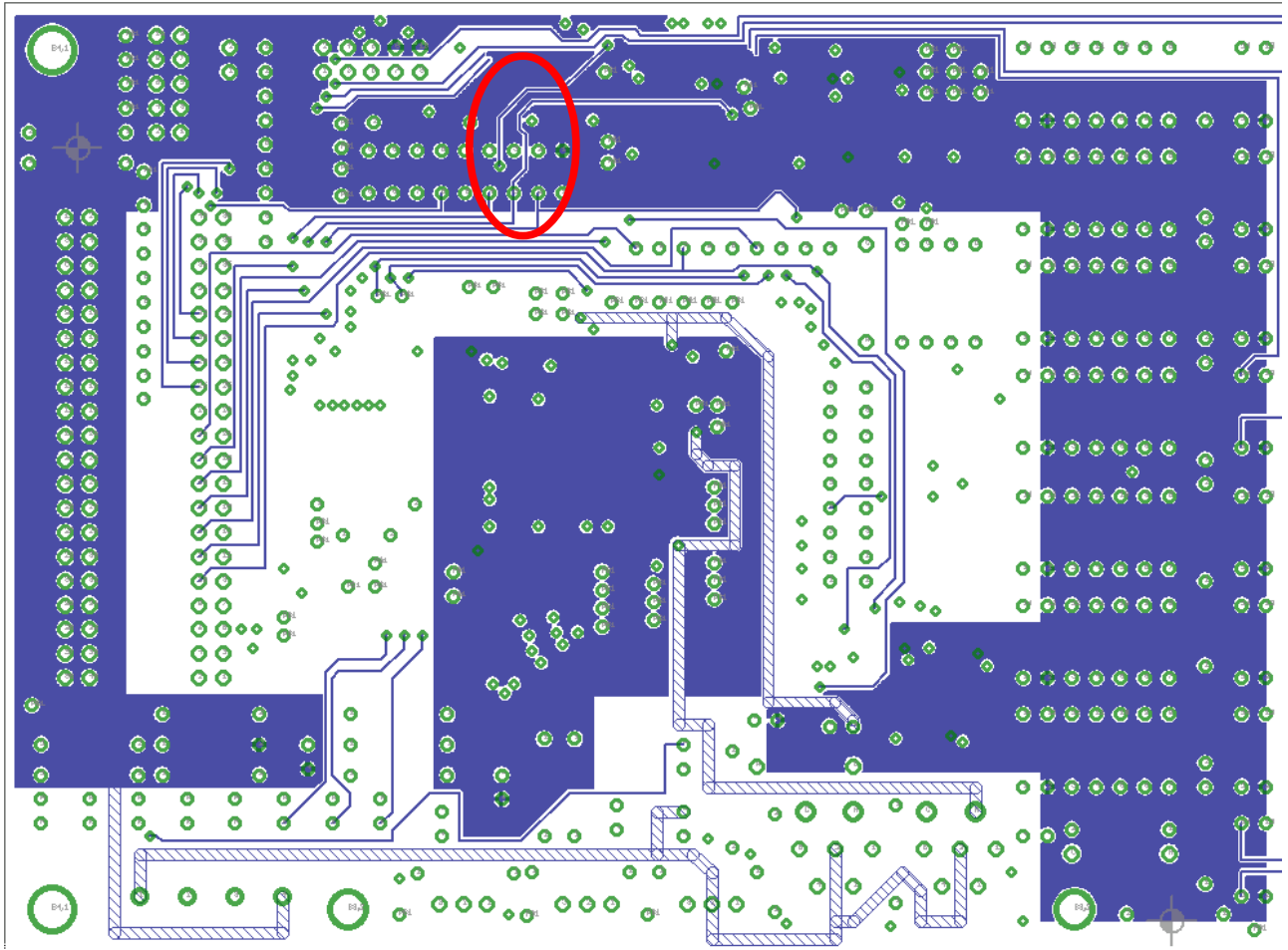
- ◆ Polygons are a great invention. By drawing a polygon in a copper layer and naming it with a signal name like GND lots of routing time can be saved.
- ◆ The **disadvantage** is: Polygons may **fall apart** during manual or automatic routing. To make sure polygons are still integer run the command "ratsnest" from time to time. The ratsnest result is shown in Drawing 24.¹¹



Drawing 24: ratsnest command

- ◆ Another critical issue are bottlenecks from one copper area to another. Drawing 25 shows an example. Red marked is a very narrow strip of copper connecting the left and the right area. This very narrow "bridge" spoils signal integrity and may be blown when carrying high currents.

¹¹ I recommend *CadSoft* to make those airwires flashing so that they can be found easily. Especially very short airwires are hard to find in large drawings.



Drawing 25: bottleneck in a polygon

3.2.3 Silk Screen Issues

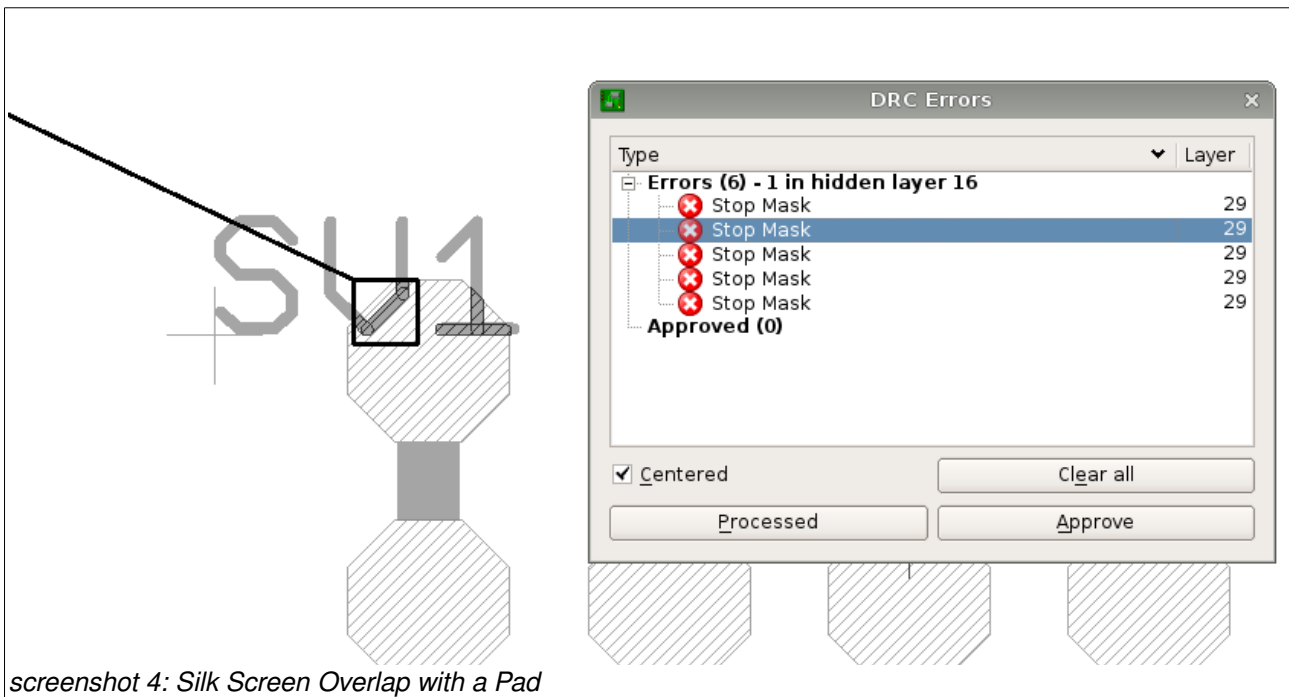
The silk screen is an option for PCBs but not a must. In general the PCB maker charges you with an extra price for silk screen. It is useful for fitting parts on the PCB and for service and maintenance as well.

3.2.3.1 Overlaps with Pads

To verify objects drawn in the silk screen layers - usually tPlace/bPlace (21/22) and tNames/bNames (25/26) – do not overlap with pads:

- display only layer tPlace (21), tNames(25) and tStop (29)
- run DRC
- display only layer bPlace (22), bNames(26) and bStop (30)
- run DRC

See example in screenshot 4 page 36.



Usually the PCB house cares for such issues by clearing the pad from silk screen data with a Gerber Editor (see page 49 point (8)). But as a good engineering practice you should care for these overlaps in the design stage.

3.2.3.2 Text Line Width (Ratio)

Please ask the PCB maker for the **minimal line width** they can guaranty. For standard PCBs 0,15mm applies in most cases.

The ratio (in %) of line width and text size and is a parameter of a text (command `info`):

$$\text{ratio} = \frac{\text{line width} * 100 \%}{\text{text size}} \quad (1)$$

Here an example: If the line must be of a width of minimal 0,125mm and the text itself is 1mm in size, the required ratio equals to:

$$12,5 \% = \frac{0,125 \text{ mm} * 100 \%}{1 \text{ mm}}$$

CAUTION: EAGLE DRC does NOT perform a line width check for structures in non-copper layers !

In other words: **The silk screen line width is not checked by DRC.**

Most frequently the text holding the name of the part (in layer `tNames/bNames`) has to be adjusted regarding its position, orientation, size and of course ratio. By default the name is hard locked to the origin of the part. Using the command `smash` this fixed connection gets broken. So I recommend following steps for the top side of the board:

- display only layer `Dimension(20)`, `tPlace (21)`, `tOrigin (23)`, `tNames(25)` and `tStop (29)`
- group all objects or run command `group all`
- smash group or run command `smash;`
- rearrange the names, adjust size and ratio (commands `move` , `group` and `change`).

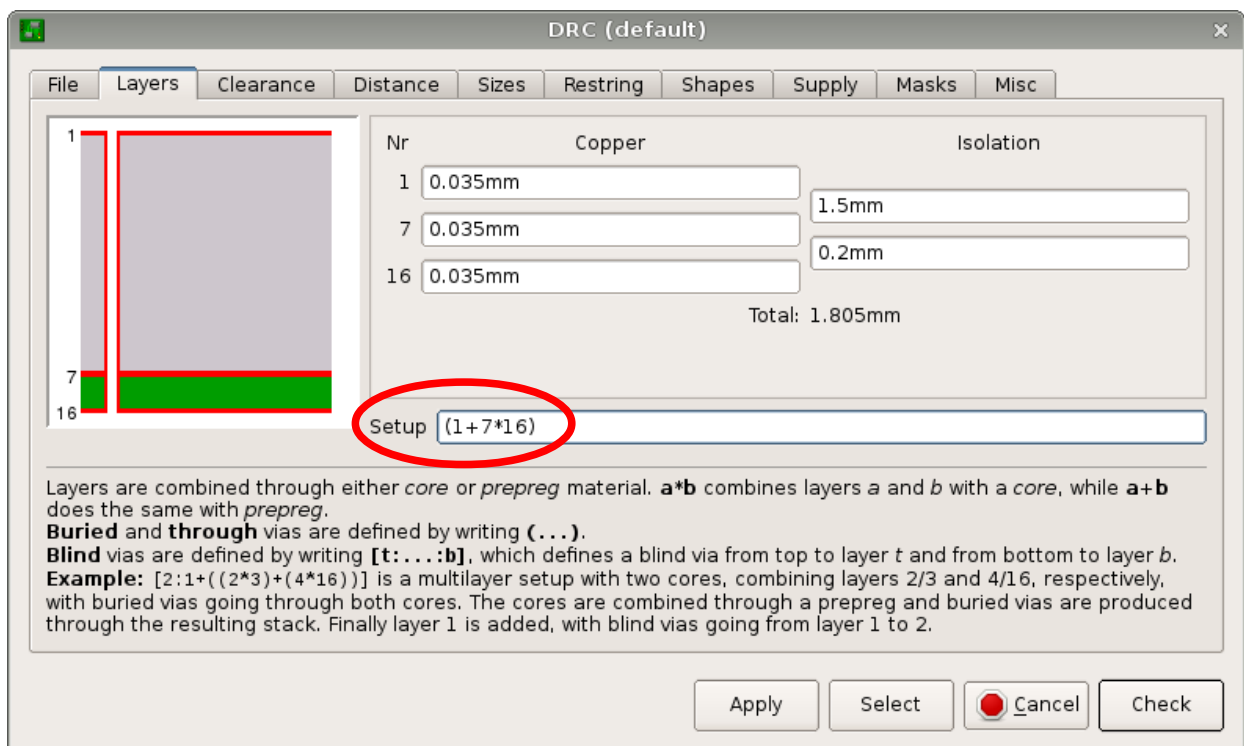
Proceed with the bottom side if required:

- display only layer `Dimension(20)`, `bPlace (22)`, `bOrigin (24)`, `bNames(26)` and `bStop (30)`
- group all objects or run command `group all`
- smash group or run command `smash;`
- rearrange the names, adjust size and ratio (commands `move` , `group` and `change`).

CAUTION: Equation 1 on page 37 implies that the smaller the text gets, the more ratio is required for the affected text.

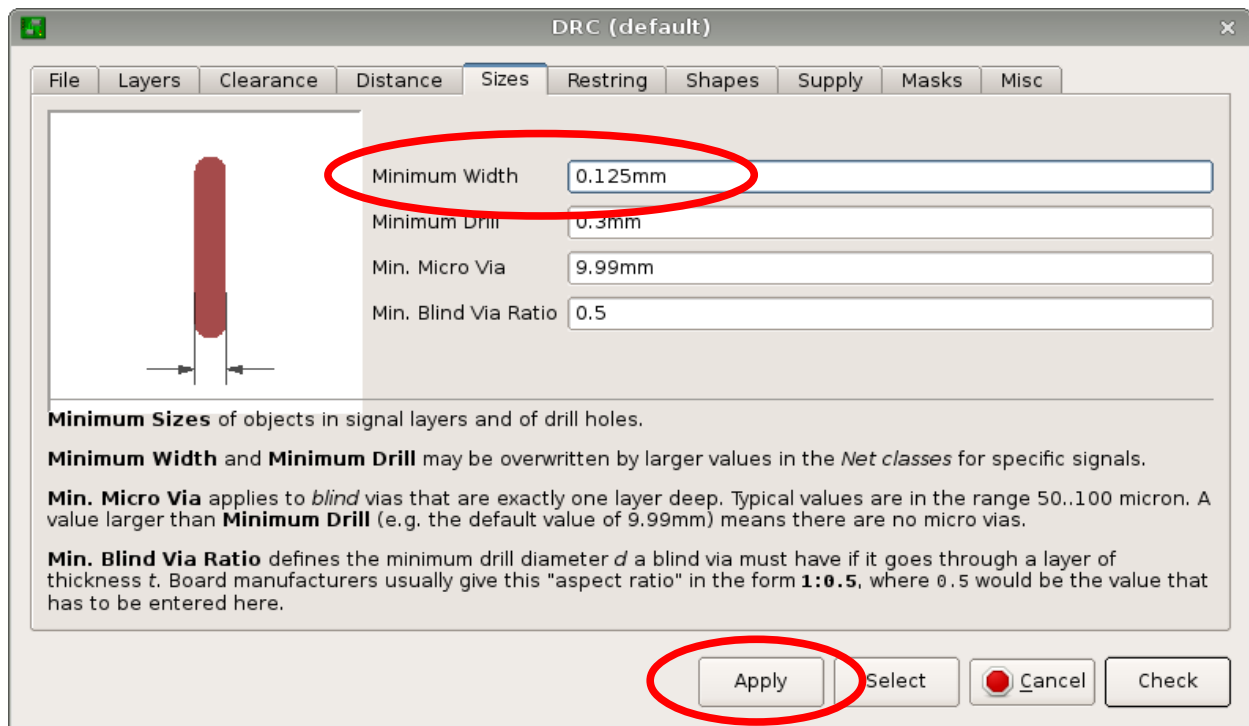
If you need to verify the minimal line width of all names, there is a workaround to force the DRC checking it at the top side of the board. Please backup your project files before proceeding with the following steps:

1. start the DRC, change into section "Layers" and invent a dummy layer as shown in screenshot 5 page 38. The layer number, in our case #7 - does not matter. The layer **must not** contain any object. Even if your board is multilayer, just create another layer. The layer limit real usable layers with this workaround is limited to 15. Of course your license must allow this step.



screenshot 5: DRC dummy layer

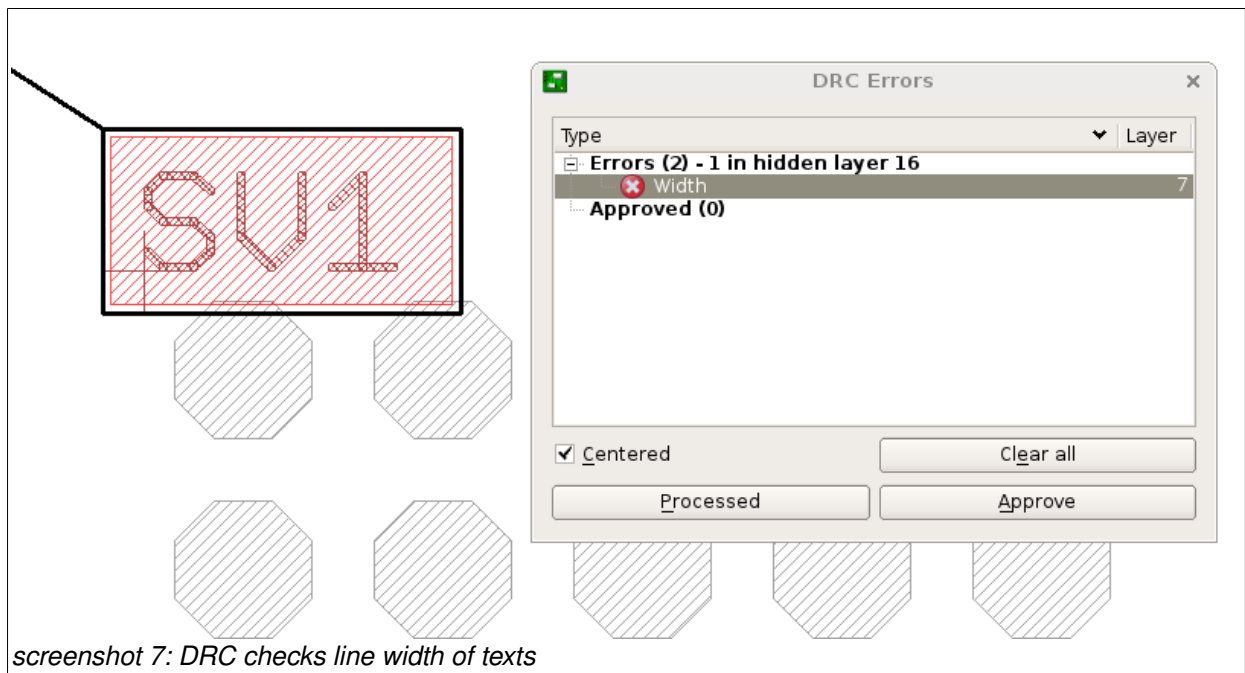
2. Change into section "sizes" and enter the minimum line width as shown in screenshot 6 page 39.



screenshot 6: DRC dummy layer sizes

3. click "Apply" and close the DRC window.¹²
4. display only layer tNames(25)
5. group all objects or run command `group all`
6. Transpose the group into your dummy layer (command `change`). By the color change the result is easy to see (screenshot 7 page 40).
7. Now run DRC again. Now that the names of the parts are in a copper layer, the DRC checks for a minimal line width of 0,125mm - in my example here. See screenshot 7 page 40. The DRC may output lots of overlap-errors which result from the texts overlapping with inner-layer vias and pads. Just ignore these errors and look for width-errors, for they belong to texts drawn with a ratio too small to meet your constraints.
8. After you have ironed out the width-errors, re-run DRC to make sure everything is fine. Then group all objects again.
9. Transpose the group back into layer tNames (25) and you are done.
10. Optional: Perform the DRC check as described in section 3.2.3.1 page 36.

¹² These dummy settings can be saved in a special dru file in section "File".



Repeat these steps for the bottom side of the board if necessary.

4 Appendix

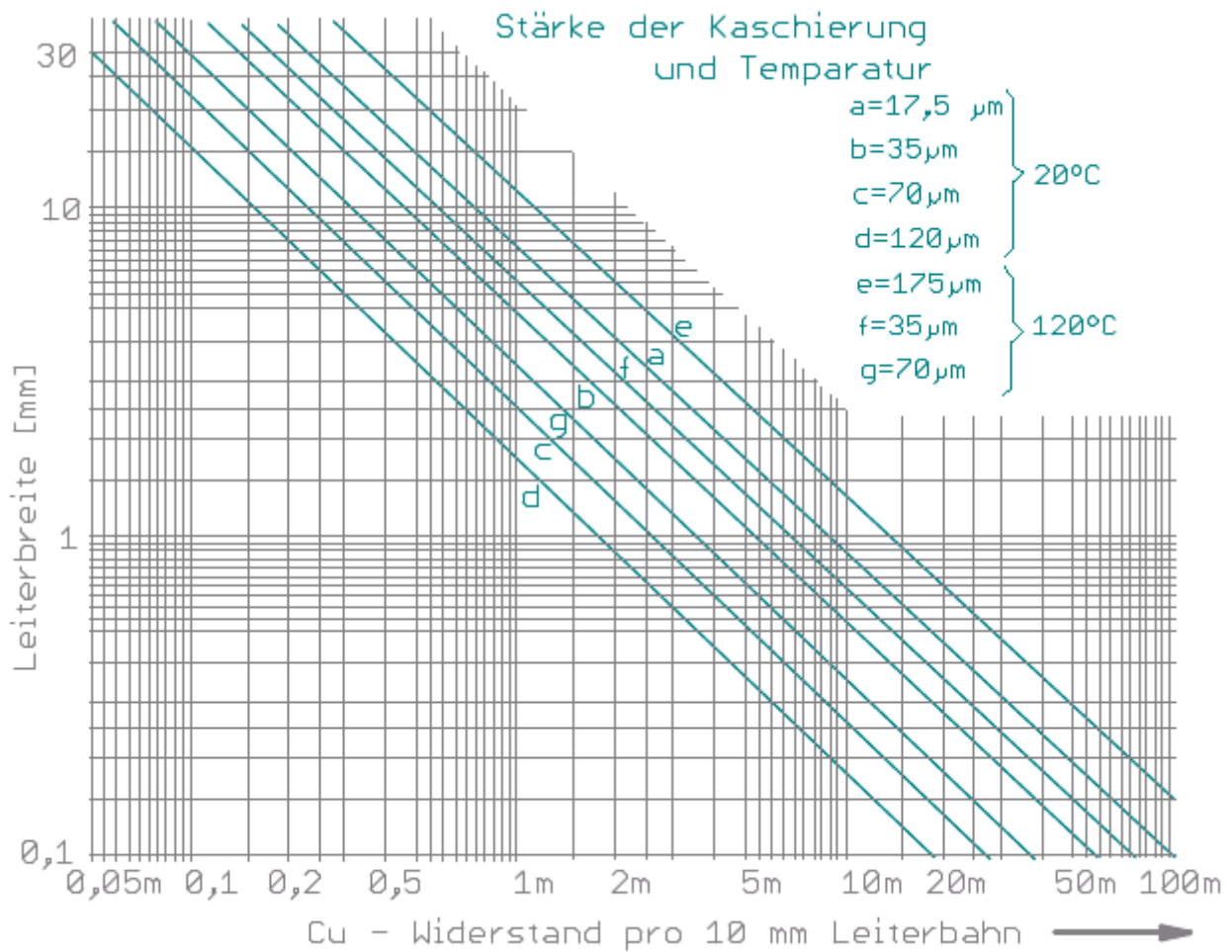


Diagram 1: maximum current load vs track width at various temperatures

German	English
Stärke der Kaschierung und Temperatur	thickness of copper coating and temperature
Leiterbahnbreite	track or wire ¹³ width
Widerstand pro 10mm Leiterbahn	resistance per 10mm track/wire length

¹³ The EAGLE terminology uses the word “wire” for all kinds of lines regardless if this is real copper or just documentation or measurement.

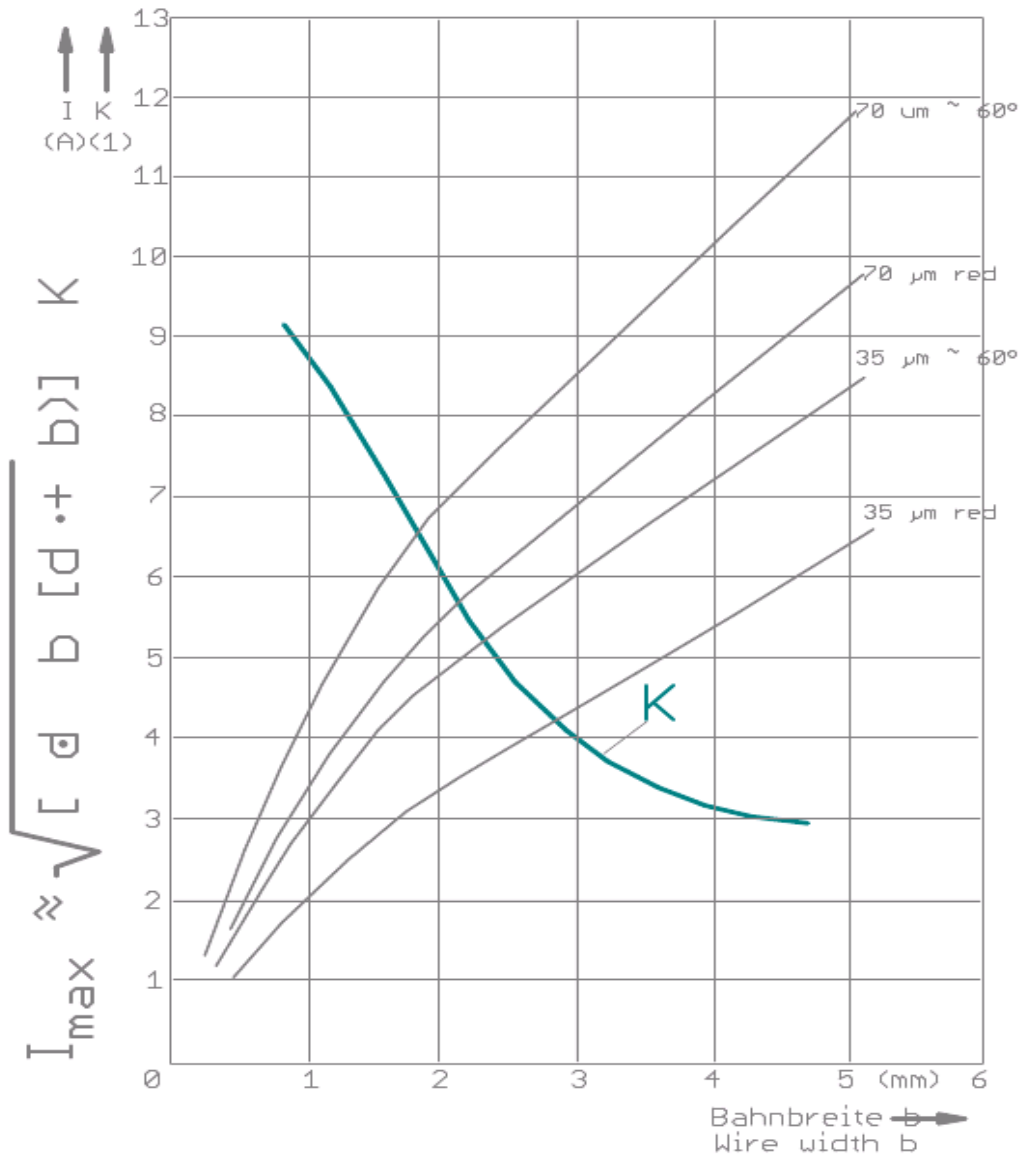


Diagram 2: maximum current load vs track width at various temperatures

Leiterbahnwiderstand

$$R = \frac{\rho \cdot l}{d \cdot b}$$

- l [mm] = Länge der Leiterbahn
- d [µm] = Stärke der Kaschierung
- b [mm] = Breite der Leiterbahn
- R [Ω] = Leiterbahnwiderstand

Metall	spez. Widerstand bei 20 °C $\left[\frac{\Omega \cdot \text{mm}^2}{\text{m}} \right]$	Temperaturbeiwert α [10 ⁻³ / °C]
Kupfer	0,0174	4,33
Silber	0,0159	4,10
Gold	0,0224	4,0
Nickel	0,078	6,75
Zinn	0,123	4,6
Blei	0,208	3,8
Palladium	0,108	3,77
Rhodium	0,0454	4,43

Beispiel :

Leiterbahnlänge l = 50 mm

$$R = \frac{\rho \cdot l}{d \cdot b} = \frac{0,0174 \cdot 50}{35 \cdot 1} = 24,9 \text{ m } \Omega$$

Kupferkaschierung d = 35 µm

Breite b = 1 mm

Table 1: track/wire resistance calculation of various conducting metals

German	English
spez. Widerstand bei	specific resistance at
Temperaturbeiwert	temperature coefficient
Leiterbahnwiderstand	resistance of track/wire
Länge der Leiterbahn / Leiterbahnlänge	length of track/wire
Stärke der Kaschierung / Kupferkaschierung	thickness of coating / copper thickness
Breite der Leiterbahn	track/wire width
Kupfer (Cu)	copper
Silber (Ag)	silver
Zinn (Sn)	tin
Blei (Pb)	lead
Beispiel	example
Breite	width

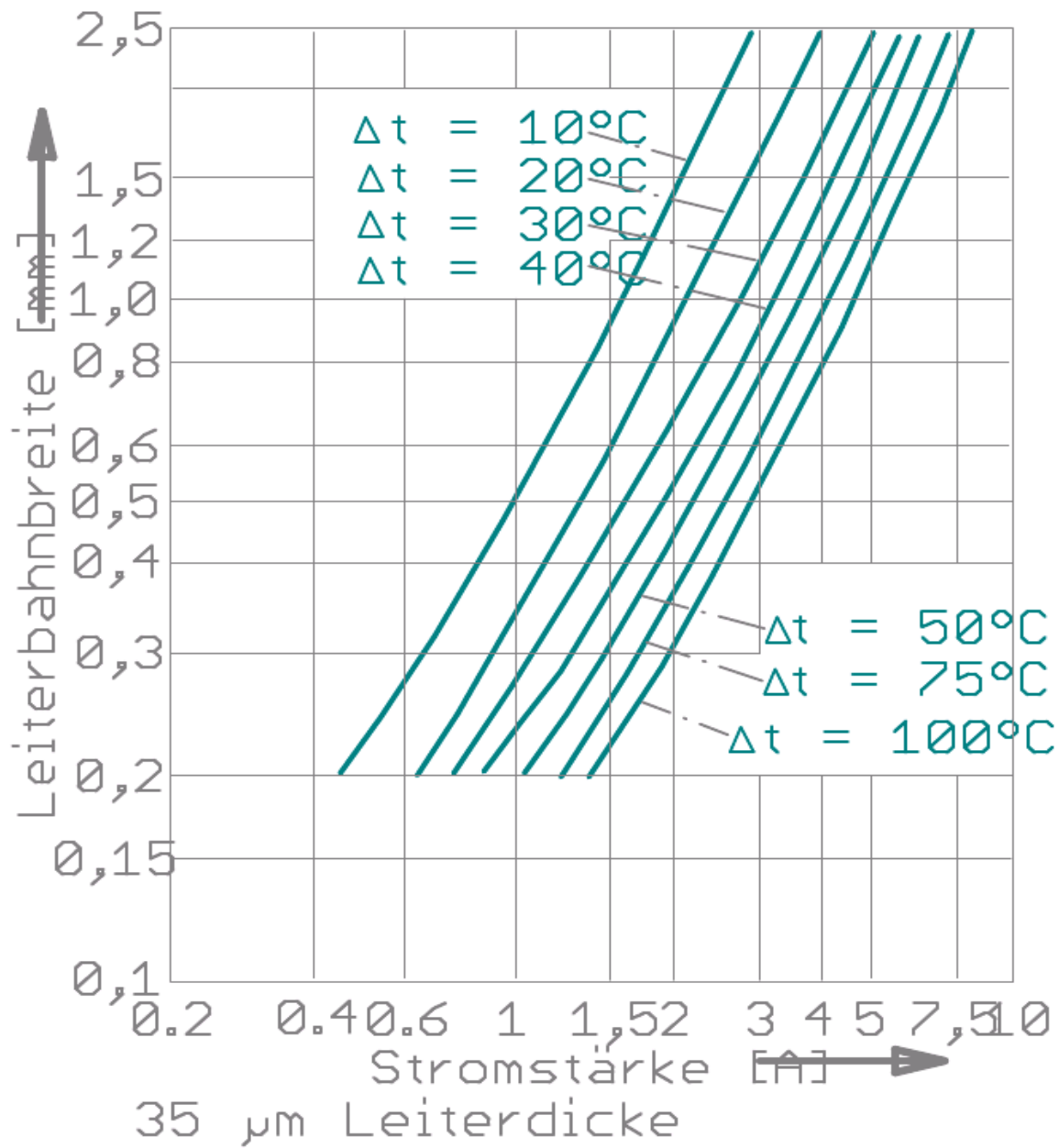


Diagram 3: maximum current load vs track width at various temperatures

German	English
Leiterbahnbreite	track/wire width
Stromstärke	(electrical) current
Leiterdicke	track/wire thickness

Isolationsabstand von Leiterbahnen

(USA MIL-Std. 275B)

A = normale Umweltbedingung

B = staubige/schmutzige Umgebung

Spannungswerte für Gleichspannung bzw. Spitzenwert der Wechselspannung

Spalte I ohne Schutzüberzug in Höhen von 0 ... 3048 m

Spalte II ohne Schutzüberzug in Höhen über 3048 m

Spalte III mit Schutzüberzug in Höhen von 0 ... 3048 m

Spalte IV mit Schutzüberzug in Höhen über 3048 m

Spannung [V]	IA	IB	II	III	IV
0 ... 50	0,381	2,032	0,660	0,381	0,559
51 ... 100			1,575		0,762
51 ... 150	0,660	2,032		0,559	
101 ... 170			3,17		1,524
151 ... 300	0,575	3,17		0,762	
171 ... 250			6,35		3,17
301 ... 500	3,17	6,62		1,524	
251 ... 500			12,70		6,35
> 500	0,0076 a Volt	0,0152 a Volt	0,025 a Volt	0,0051 a Volt	0,0127 a Volt

Die angegebenen Zahlen sind Mindestwerte in mm.

Table 2: clearances between tracks/wires

German	English
Isolationsabstand von Leiterbahnen	clearance between tracks/wires
normale / staubige / schmutzige Umweltbedingung	normal / dusty / dirty environment
Spannungswerte für Gleichspannung bzw. Spitzenwert der Wechselspannung	DC voltage or AC peak voltage
Spalte	column
ohne/mit Schutzüberzug in Höhen von/über x m	with/without protective coating at altitudes of/above x Meters
Spannung	voltage

Die angegebenen Zahlen sind Mindestwerte in mm.	Numbers given are minimal values in Millimeters .

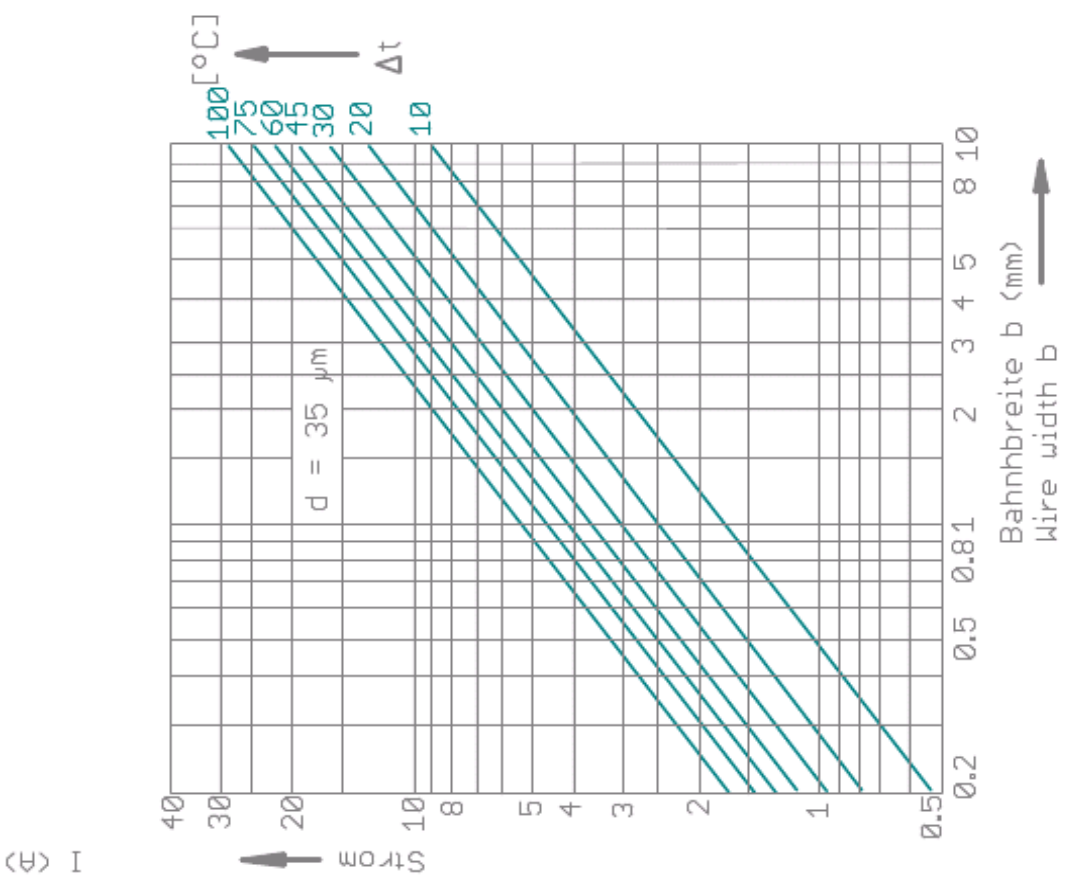
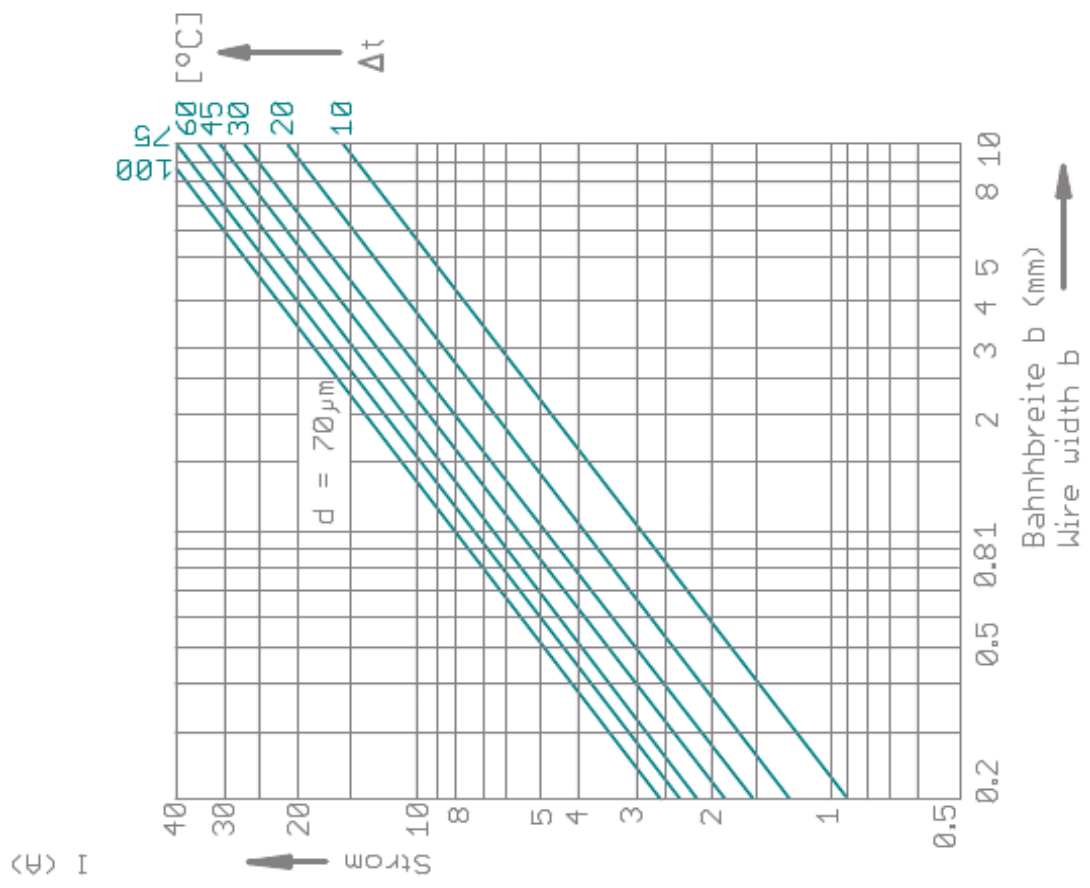


Diagram 4: maximum current load vs track width at various temperatures

5 Useful Links

- (1) *CadSoft EAGLE Training and Consulting* – a reasonable way to reasonable work at <http://www.train-z.de>



- (2) An *EAGLE* configuration script [eagle.scr](#) . Units, grid, line with, text size, font, drills and more – well defined and cleaned up ...

- (3) Find updates of this checklist at <http://www.train-z.de>

(4) [What is Boundary Scan ?](#)

(5) Looking for a lean [Boundary Scan Test System](#) ? Please have a look [here !](#)

JTAG/Boundary Scan System M-1
according to Std. IEEE 1149.1

- **Minimal** UUT access via **5 wire** IEEE1149.1 test bus
- Fault diagnosis down to pin level
- Interconnect Test (short/open detection)
- Memory-Connect Test (RAM/ROM/FLASH)
- Oscillator Test / Clock Test
- LED, Display Test, Logic Test ...

- UUT Power Switch and Monitoring up to 6A / 48 V DC
- full galvanic separation of UUT from Scan Master in Non-Test Mode
- Operator Activity reduced to pushing START / STOP Button
- PASS / FAIL display by just two front panel LEDs

Contact: Mario Blunk / Blunk electronic / Buchfinkenweg 5 / 99087 Erfurt / Germany
info@blunk-electronic.de / www.train-z.de / Phone +49 361 518 9618 / +49 176 290 45 855

(6) Debug SPI, I²C, Boundary Scan/JTAG and other hardware with the *Logic Scanner* at http://www.train-z.de/logic_scanner/index.html

- (7) *EAGLE* - an affordable and very efficient schematics and layout tool at <http://www.cadsoftusa.com>



- (8) A Gerber Data Viewer and Editor at <http://www.pentalogix.com>

German Sales and Support Office:

Helmut Mendritzki
Software-Beratung-Vertrieb
Dahlienhof 1
25462 RELLINGEN
GERMANY
Tel.: +49 (0) 4101 - 20 60 51
Fax: +49 (0) 4101 - 20 60 53
Mobile: +49 (0) 171 - 2155852
eMail: mendritzki@aol.com



- (9) The office alternative : *LibreOffice* at <http://www.libreoffice.org>



6 References

- (1) Mario Blunk, “*EAGLE Library Tutorial*” at http://www.train-z.de/pdf/library_tutorial.pdf
- (2) Joachim Franz “*EMV Störungssicherer Aufbau elektronischer Schaltungen*” ; German; ISBN 978-3-8348-0893-6
- (3) *CadSoft EAGLE* Version 6.x English users manual
- (4) Stencil Design Guidelines IPC-7525A, February 2007
- (5) Hans-Joachim Fischer / Wolfgang E. Schlegel, “*Transistor- und Schaltungstechnik*” ; German; ISBN 3-327-00362-9
- (6) The Institute of Electrical and Electronics Engineers, Inc. , 3 Park Avenue, New York, NY 10016-5997, USA; IEEE Std 1149.1-2001 “*IEEE Standard Test Access Port and Boundary-Scan Architecture*”
- (7) Mario Blunk, “*A Guide to test methods and why to go for Boundary Scan*” at http://www.train-z.de/bsm/how_to_test.pdf

7 Disclaimer

This document is believed to be accurate and reliable. I do not assume responsibility for any errors which may appear in this document. I reserve the right to change it at any time without notice, and do not make any commitment to update the information contained herein.

My Boss is a Jewish Carpenter

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