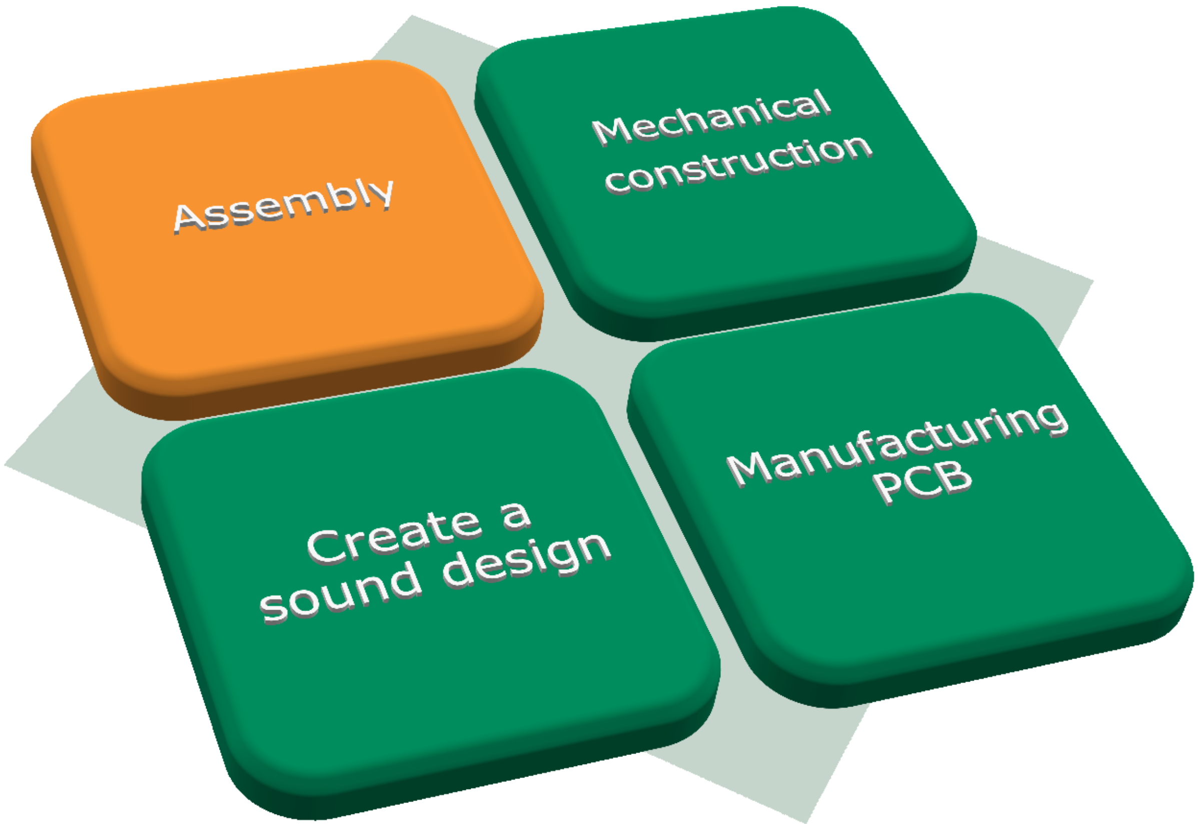
PCB Design considerations

Better product
Easier to produce
Reducing cost
Overall quality improvement

PCB design considerations



PCB Design to assure optimal assembly

- Place at least 3 fiducials (global fiducial) on the PCB per SMD side. (spot diameter 1,5 mm)
- In the soldermask keep a space free; 4,5 mm a circle or a square. The free space should be free of copper or just complete copper.
- All the SMD-parts should be within the capture-area of the fiducials
- For very small parts and BGA 2 local fiducials should be added (0,8 or 1 mm). In the soldermask an area of 3x times the spot diameter should be kept free
- In case of a large PCB it is suggested to divide the area in smaller areas, and add additional fiducials

PCB Design to assure optimal assembly

- Components should be placed at least 5mm from the PCB outline (for the PCB sides used to clamp the PCB)
- For conventional parts 5 mm – SMD 3 mm
  This way the PCB can be clamped in a proper way by the automatic assembly line
  Otherwise the risk exists that the parts within the 5mm border need to be placed by hand
- Optional: make use of a break edge (or Panel)

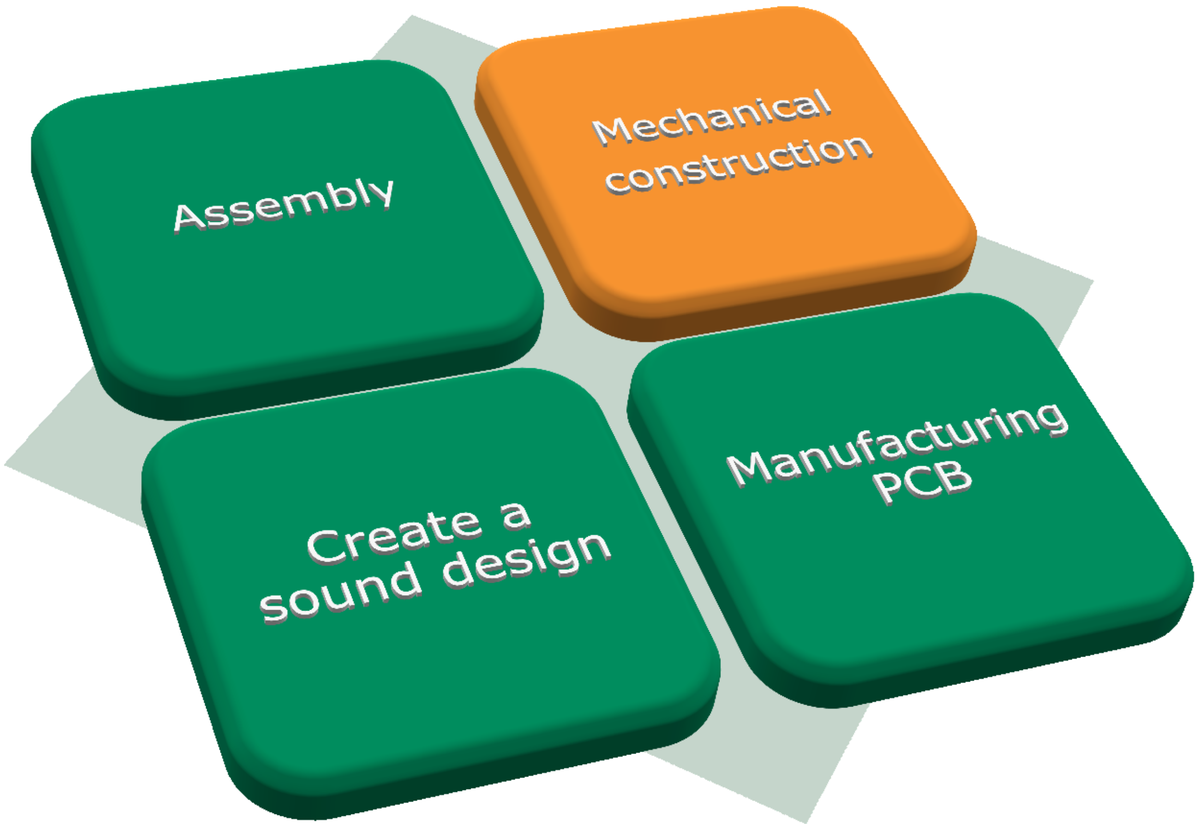
PCB Design to assure optimal assembly

- Polarities; preferably all in the same direction
- Press fit technique
  Use of press fit preferable NOT in combination with Immersion NiAu (Enig), better with HAL / HAL PBfree.
  Always keep sufficient area free for the press fit tools
- Reduce the risk of bad solder joints
  - Well balanced copper distribution over the PCB.
  - A high amount of copper at the component side will absorb too much heat, resulting in bad solder joints.
- Vias should they be block or not?
  In general no blocking.
  Never block the vias at the Reflow-Site!

PCB Design to assure optimal assembly

- When no solder mask is applied, for some special reason (HAST-tests pe.) Adding of small solder dams at the outgoing tracks will prevent that the solder will flow away
- Create stencil masks with a 1:1 ratio; the assembly shop will adjust the mask in case needed
- In case of multiple PCBs (Panels) contact the assembly shop first to assure that the dimensions are correct
- Keep sufficient free space in case of partial wave soldering. No SMD at PTH pinning. (minimal 4mm distance)

PCB design considerations



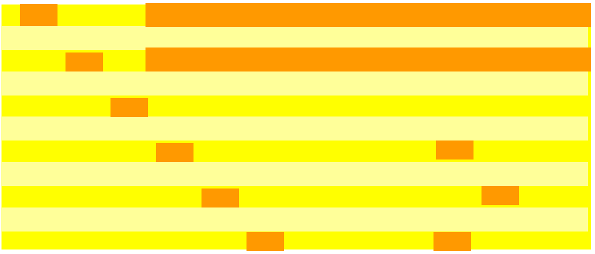
PCB design avoiding mechanical issues

- Tracks should be minimal 1 mm from the edge of the PCB.
- V-cut ⬄ Routing
  V-cut is not possible with Teflon material!!!
- Holes can be max 2,8mm using peel mask
- For countersunk holes check for sufficient (isolation)distance between the hole and the innerlayer. *Often it is observed that the copper of the innerlayer is touched by drilling the sunk holes.* (Shortcut risk!!!)

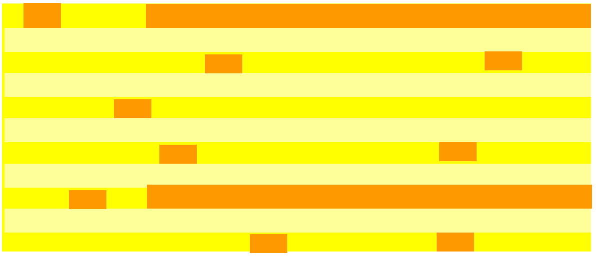
PCB design avoiding mechanical issues

- In case the final thickness of a PCB is very critical;
  Mark on the drawing the overall thickness and its tolerance
  Bear in mind that tight thickness control in the production process of PCBs is difficult (risk of increased cost)
- Asymmetrical build can result in bow and twist of the board.
  - Optional: add a dummy layer.

PCB cross section
Marginal copper distribution
Risk for bow



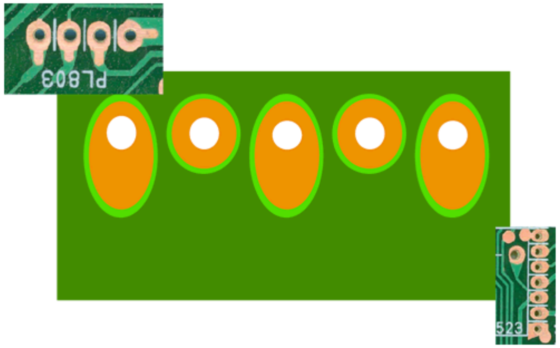
PCB cross section
Distribution of Copper OK
No risk for bow



PCB design considerations

PCB Design to assure optimal PCB production

- Via-holes always according the manufacturing instructions. (Aspect ratio)
  Too small holes will result in unreliable plating thickness and will result in increased manufacturing cost
- Pad / hole ratio should be OK (hole + 0,5 mm is standard)
  For VHDI-PCB other ratios could be used; always contact the manufacturer first
- In case of hard gold: no isolation distances < 0,15mm for the hard gold.
- Apply teardrops at the outgoing tracks for the very small tracks.

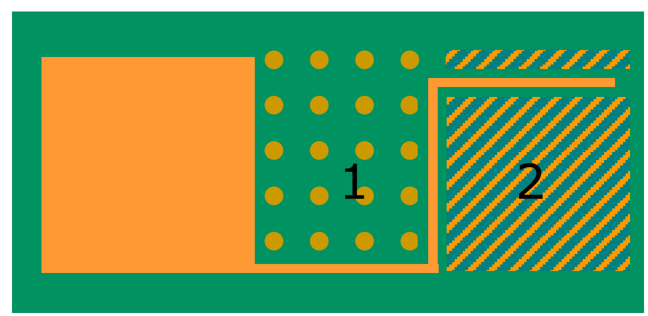


PCB Design to assure optimal PCB production

- Pay attention to have an evenly distribution of the copper on all layers of the PCB. When needed; add additional copper (copper structure). This will also improve the etching process and will help to avoid bow of the PCB
  - Basic rule: maximum 50% ratio difference in copper coverage

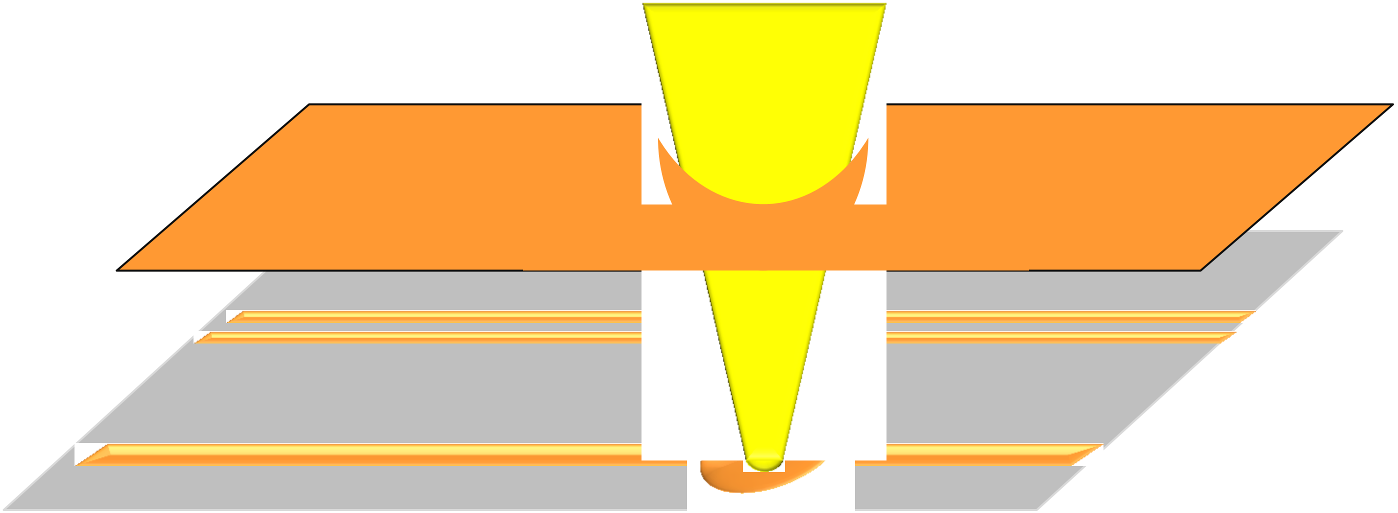
Less preferred
- Unequal distribution of CU
- Reason for PCB with bow

Possible solution
- Adding of extra Cu structure
- Pattern free to choose (1,2)

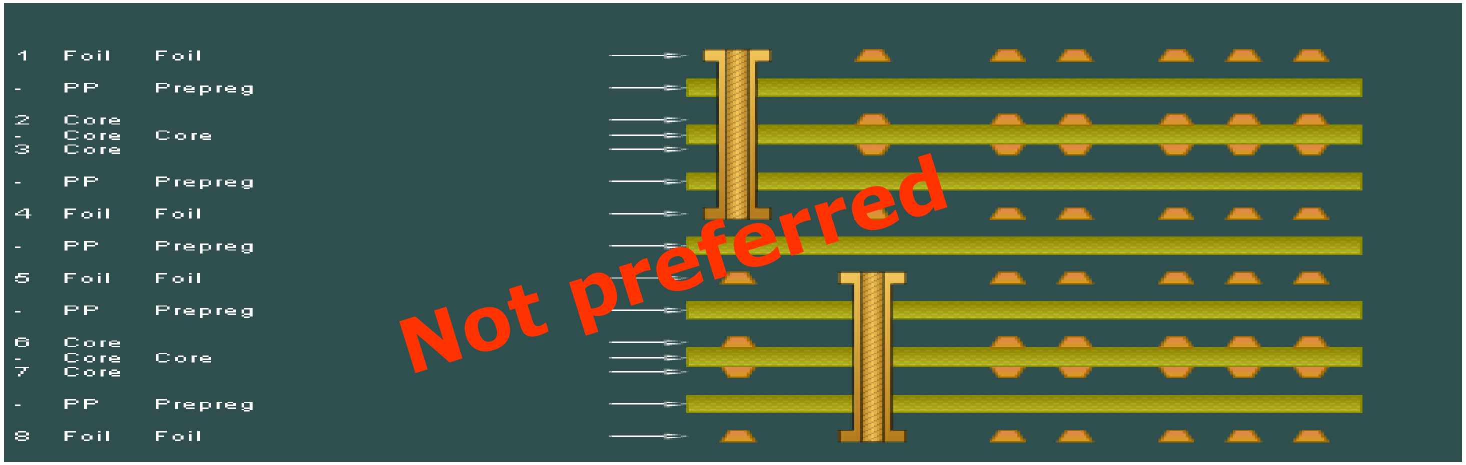


PCB Design to assure optimal PCB production

- When applying a laser made blind via, ensure that the copper area in the innerlayer is large enough. This to ensure that the laser will hit the copper area reliably during production

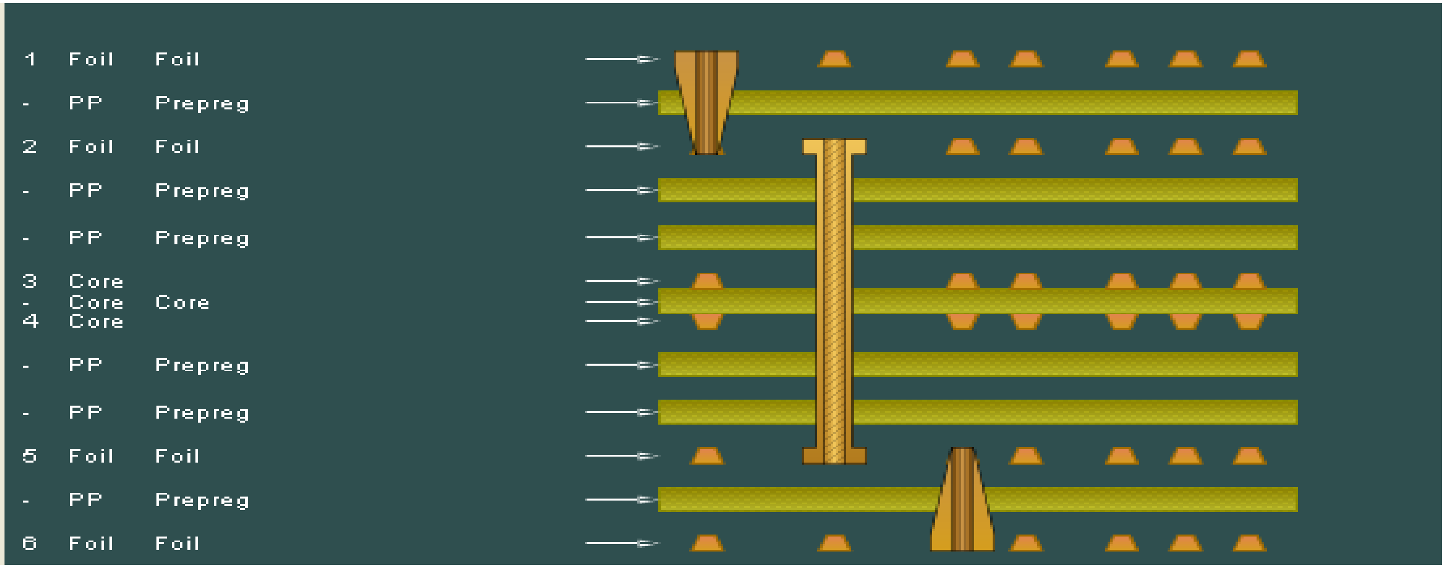


PCB Design to assure optimal PCB production

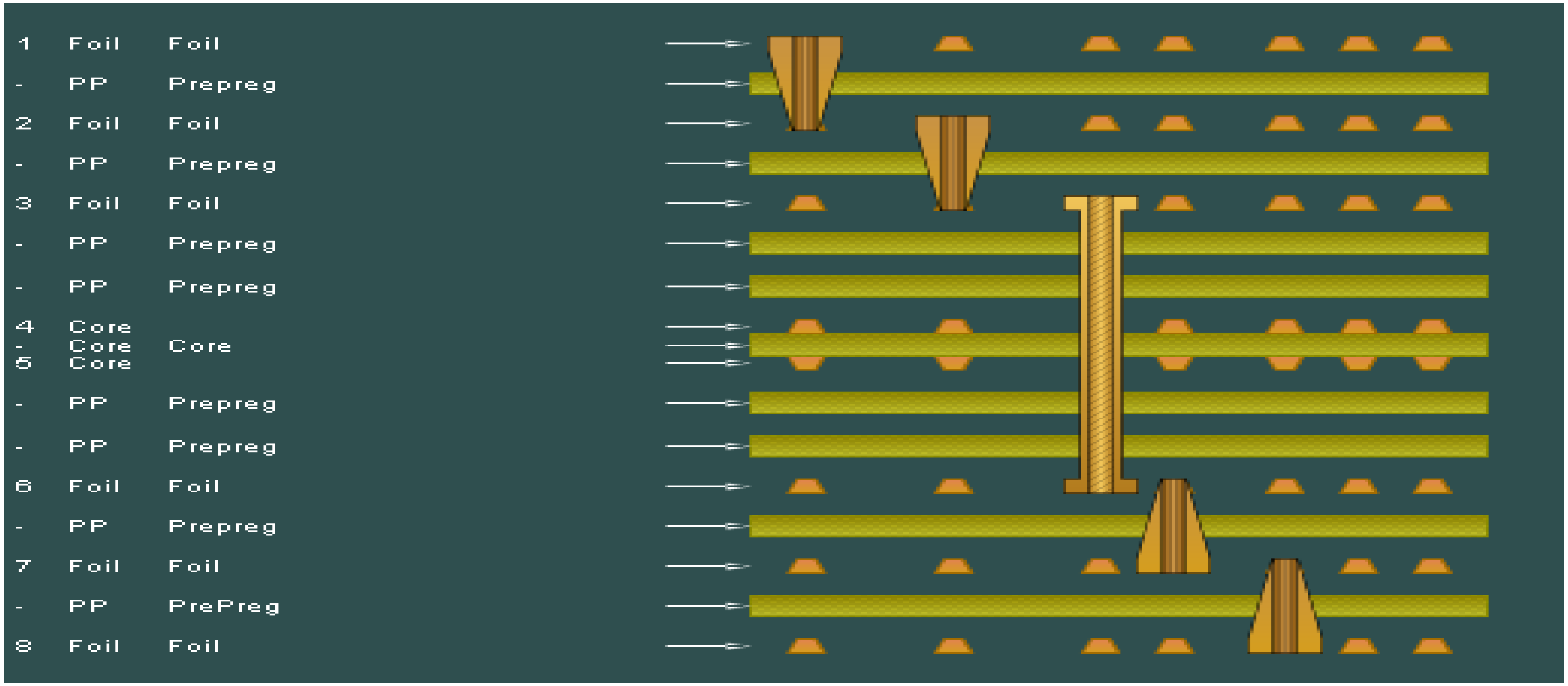


- Sample of a typical 4+4 build
- The build are 2 4-layer PCBs connected with each other
- The two parts can not be tested individually before they are connected with each other
- 2 Press cycles
- Registration of the layer build is critical
- Backside filled vias are needed

PCB Design to assure optimal PCB production



- Sample: Typical 1+4+1 build
- Build of 2 till 5 is equal to a standard 4 layer Multilayer
- The build of layer 2 till 5 can be tested before layer 1 and 6 are added
- 2 Pressing cycles



- Sample of a typical 1+1+4+1+1 build
- The assembly of Layer 3 till 6 is as a standard 4 layer Multi-layer
- The assembly of Layer 3 till 6 can be tested before the outerlayers are fitted
- 3 pressing cycles
- Registration of layer 2 and 7 is critical

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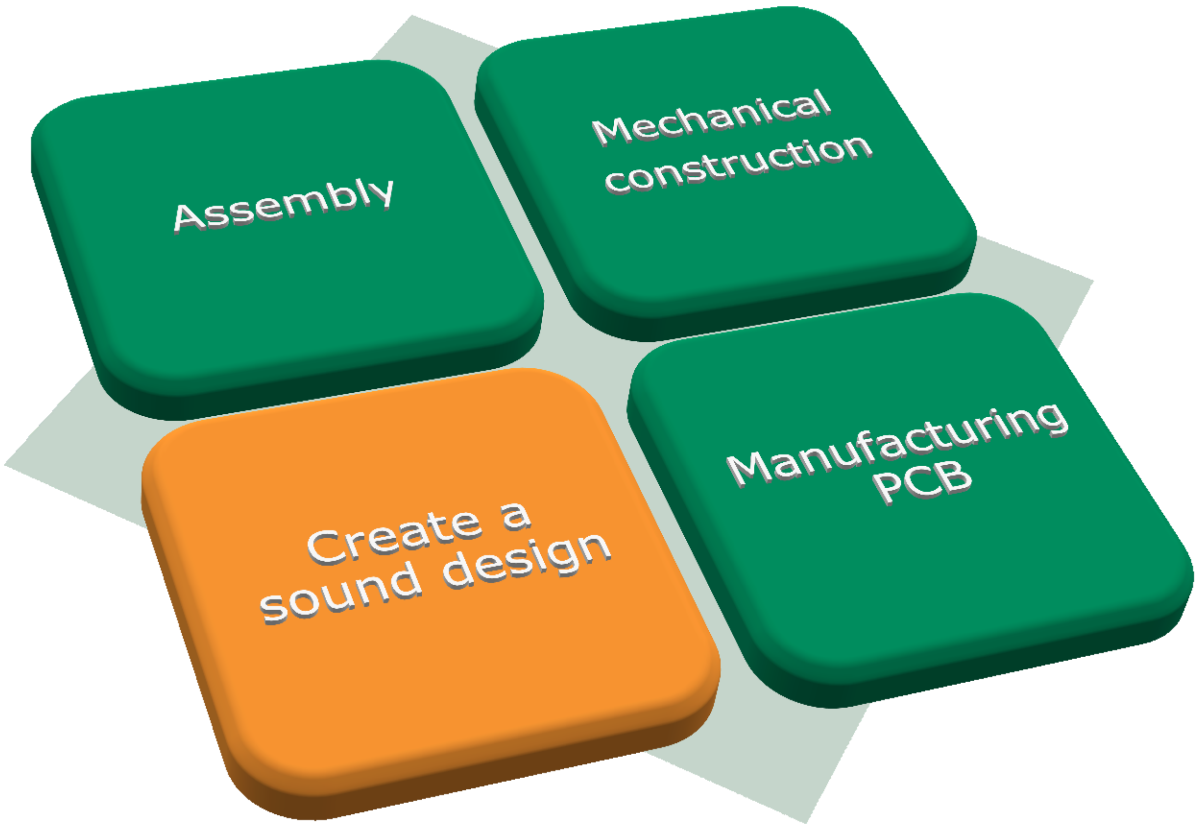


Create a solid PCB design

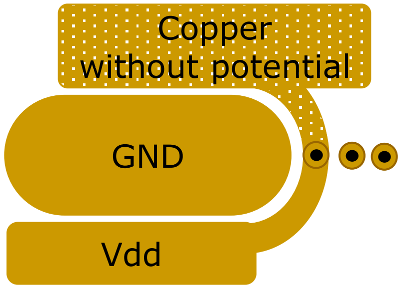
- Hole diameter for conventional parts should be minimal: wire thickness +0,2 – 0,3mm
- By wave-soldering: always place the parts in the correct transport direction.
  Do not place large (high) components in front of small (low) components.
  Keep the shadow effect in mind!!
- Considering HAL ↔ Immersion NiAu
  In case of small isolator distances always apply immersion NiAu. The pads have a smoother surface compared to HAL. The result: Less chance for shorts after soldering. The shelf life of Immersion NiAu is longer. Pads are more flat, easier to solder fine pitch components.

Create a solid design

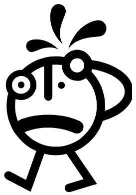
- Always use a sufficient number of vias to ensure proper current supply
- Maximum currents
  via 0,3mm - 1,0 amp
  via 0,5mm - 1,5 amp
  A few smaller vias are preferred over one big via
- When special impedance is required: always mark this clearly on the drawings, also note this at the RFQ stage
- As an option; routing holes can be plated
  For high vacuum applications the PCB edge can also be plated to avoid outgassing through the PCB material

Create a solid PCB design

- Application of immersion thick gold; should always be marked very clearly and detailed in the engineering documents
- For the lay-out program, preferable define the use of a infinite small grid
- Do not apply copper without potential



- Tracks in the inner layers transporting high currents should be 2 – 2,5 x wider compared to the outer tracks under same conditions due to the lesser cooling



Create a sound PCB design

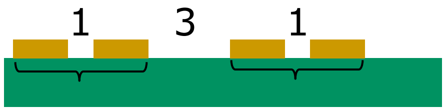
- Critical tracks like:
  - Clock
  - Data-bus
  - Interface

  Should always be lay-outed manually

- The supply current preferably distributed with a low resistance copper area in the layer

Create a solid PCB design

- For high vacuum applications the PCB should be gold plated for sufficient flatness
- A soldermask can not be used in combination with a high vacuum application.
- 3x times the isolator distance should be applied between 2 sets of differential pair of tracks



- don‘t apply cross tracks due to the risk of a jump in impedance at a potential jump

Create a solid PCB design

- Don’t place an array of vias next to each other to avoid the risk of a ground-loop
- Earth track at the outer side of the PCB: around drilling and create vias. Those vias could have fixed have distances to each other. At the inner side of the PCB the vias should be applied making use of an irregular grid

Do you miss something?

- Q.P.I. has tried to give a complete overview of important design considerations. Do miss one, please let us know. We can add it to the list.
- Contact qpiinfo@qpigroup.com

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Q.P.I. Group B.V.
Schootense Dreef 27
5708 HZ Helmond
Netherlands

T +31 (0)492-590 059, direct dial
E qpiinfo@qpigroup.com