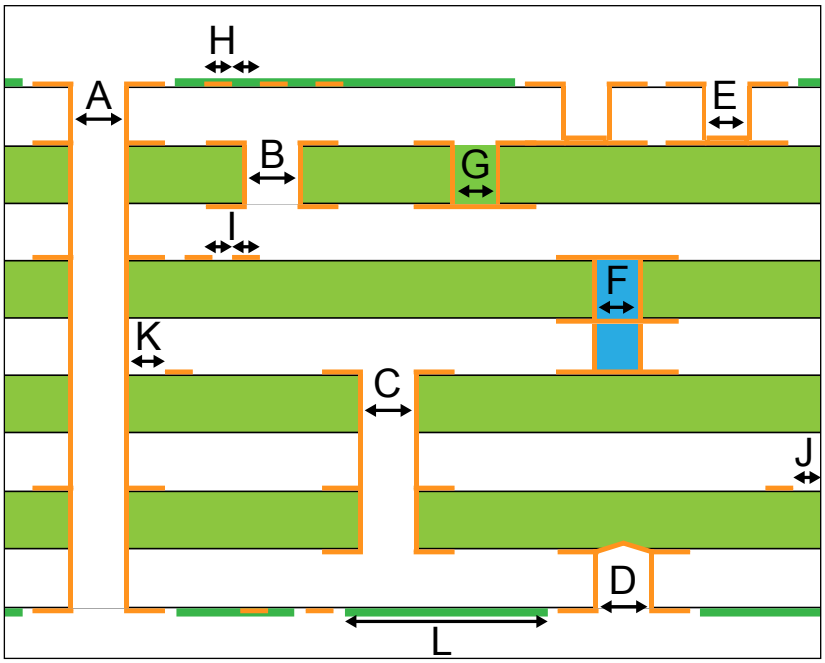
multi-cb
PRINTED CIRCUIT BOARDS

BASIC DESIGN RULES

1. Design Parameters

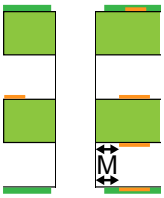


Inner layers: conductor / copper thickness		
copper thickness	**conductor trace -width / spacing**	**annular ring min.**
12µm	75µm*	100µm
18µm	100µm	100µm
35µm	125µm	100µm
70µm	200µm	200µm
105µm	250µm	250µm
140µm	300µm	300µm

Outer layers: conductor / copper thickness		
copper final-thickness	**conductor trace -width / spacing**	**annular ring min.**
30µm	75µm*	75µm
35µm	100µm	100µm
70µm	200µm	200µm
105µm	250µm	250µm
140µm	300µm	300µm
210µm	500µm	500µm
400µm	900µm	900µm

Name			Dimensions min.			
			aspekt ratio	final-Ø	via-pad	annular ring
A, B, C	via, buried via		1:12	75µm	225µm	75µm
D	blind via, mechanical	max. Ø 400µm	1:1	100µm	400µm	150µm
E	blind via, laser		1:1	75µm	225µm	75µm**
F	stacked vias Should be avoided, due to it`s disproportionately high use of time and effort. Please contact always our CAM department for alterna-tives.		1:1 Ø < 100µm 1:4 Ø ≥ 100µm 1:10 Ø ≥ 150µm 1:12 Ø ≥ 200µm	100µm	300µm	100µm
G	staggered vias		1:1 - 1:12 (Øs.o.)	100µm	300µm	100µm
H, I	conductor traces outer, inner		width space		75µm 75µm	
J	conductor, pad <> milling edge conductor, pad <> scoring edge		space space		200µm 500µm	
K	conductor, pad <> via		space		200µm	
L	solder-stop coating		clearance bridge width		50µm annular 100µm	

*** Depending on the design,** please clarify in advance! ****** Min. annular ring **depends on the copper thickness**! Please check for critical designs.



NPT - Holes

min. Ø: 200µm
max. Ø: 6,0mm (bigger = milling)
aspekt ratio: 1:10 (a.A. 1:12)

M conductor, pad <> NPTH: min. 150µm

Pilot or mounting holes (usually with Ø = 3,05mm) should be created in the same drill program as NPT-holes. Please label mounting holes in the dimension layer, as such.

Coil

Coils on the inner layers need a min conductor -width / -space of 125µm.
Coils on the outer layers need a min conductor -width / -space of 100µm.

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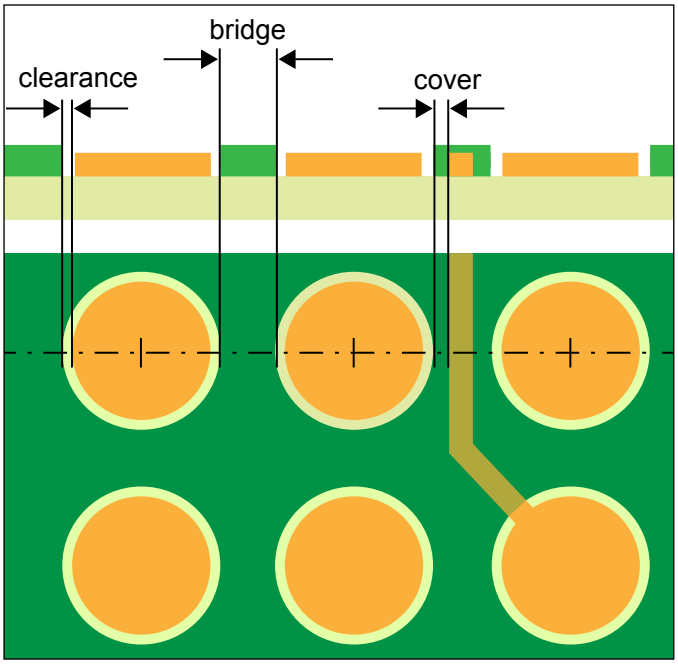
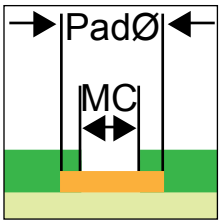
2. Solder-stop



Solder-stop = green		
	standard	**on request (data)**
clearance	50µm	40µm
bridge width	100µm	80µm
cover	100µm	80µm

Solder-stop <> green (black, blue, white, red)		
	standard	**on request (data)**
clearance	75µm	40µm
bridge width	150µm	100µm
cover	150µm	100µm

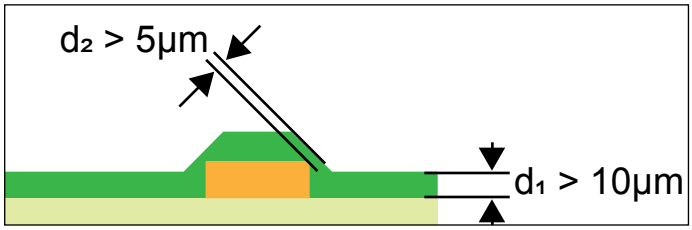
SMD-Pads (Solder-Mask-Defined Pads)



For solder pads, which are defined by the solder-mask, please use the following parameters:

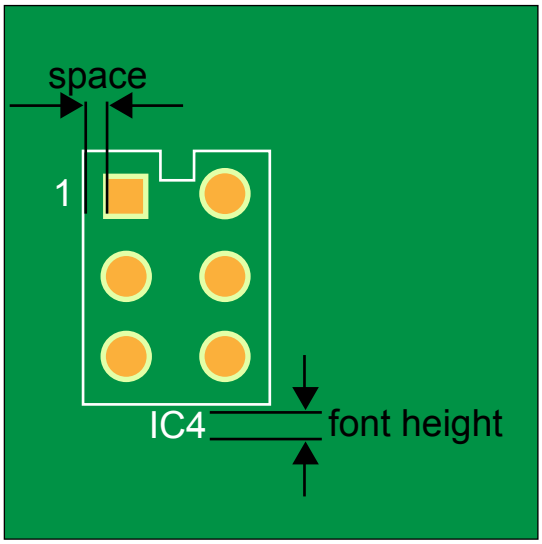
MC Ø (Mask Clearance) = Pad Ø - 80µm

Process capable for drill Ø ≥ 0,3 mm



Solder-stop Parameters	
	thickness
d1: on the PCB	> 10µm < 25µm
d2: on the conductor edge	> 5µm < 25µm
electric strength	500VDC min.

3. Marking print



Marking Print Parameters		
font height	**ideal font width**	**min. font width***
1,2mm	150µm	100µm
1,5mm	180µm	125mm
1,8mm	200µm	150µm
spacing to pad min.	150µm	
spacing to solder-stop clearance	100µm	
Never place marking print on pads > will be clipped by Multi-CB befoe production.		

* Can lead to surcharge

For EAGLE-Users

Before exporting your data, you should always activate the option

- “Always vector font”

which is found under: Options/User interface. Otherwise your marking print will very probably be incorrectly applied (EAGLE V. 5).

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4. Tolerances and Design Limits

The production of printed circuit boards is carried out according to the valid IPC guidelines and standards and on the basis of following technical specifications. HDI or MFT boards can be produced with smaller tolerances. Differing requirements of the customer must be explicitly agreed!

Pattern tolerances	
	Tolerance
Drilling (PTH) to conductive pattern outer layers	±0,10mm
Drilling (PTH) to conductive pattern inner layers	±0,15mm
Drilling (PTH) to milling pattern / contour	±0,10mm
Drilling (NPTH) to milling pattern / contour	±0,10mm
Drilling (PTH) to marking print	±0,15mm
Conductive pattern to solder resist	±0,10mm
Conductive pattern to marking print	±0,20mm
Hole to hole, one pass* PTH-PTH or NPTH-NPTH	±0,05mm
Hole to hole, two passes PTH-NPTH	±0,10mm
* Also applies for PTH-NPTH if they are drilled in one run (e.g. location holes for SMD stencils)	

Conductor (acc. to IPC-6012C)		
Conductor width	min. 80%	in comparsion to the data
Conductor space	max. 30%	reduction in comparsion to data

Impedance control	
Tolerance (normal)	10%
Tolerance (extended)	5%

Milling	
	Tolerance
Milling offset	±0,10mm
Z-Axis milling depth	±0,20mm

Base material	
	Tolerance
FR4 thickness	±10%
The information about the base material thickness exclusively defines the thickness of the dielectric including base copper. The other layer structures such as electroplated Cu layers or solder resist layers result in increased final thickness.	

Vias & Drills		
		End-Ø
Plated-through-holes (PTH) and component holes	HAL surface	±0,10mm
	chemical surface	±0,05mm
Non-plated-through-holes (NPTH)		±0,05mm

Cu min. thickness of throughplating		
	Class 2*	**Class 3**
Via (> 150µm)	20µm - 25µm	20µm - 25µm
Microvia (≤ 150µm)	18µm - 20µm	20µm - 25µm
Blind Via	10µm - 12µm	10µm - 12µm
Buried Via	10µm - 12µm	10µm - 12µm
* Standard		

Scoring	
	Tolerance
Offset (to PCB center)	±0,10mm
Drilling (PTH) to scoring pattern	±0,15mm
Drilling (NPTH) to scoring pattern	±0,20mm
PCB dimension x/y	±0,15mm
Scoring depth	±0,20mm

Bow & Twist	
	Tolerance
For PCBs ≥ 0,8mm thickness	0,75% with SMD
	1,50% without SMD
Please note that the twist & bow value is increased above average, if the copper balance of the PCB is locally very unequal or if the circuit board is very thin.	

Delivery quantity	
	Tolerance
Excess or short deliveries of up to	10%